Ge NW FETs Fabrication

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Germanium is attractive for the future technology node application because of its two times higher electron mobility and 4 times higher hole mobility than that of Si counterpart. . The lower band gap of Ge also allows the supply voltage scalability to satisfy the post-Si CMOS era. How-ever, the Ge MOSFET tech-nology is facing several serious challenges, including fast n-type dopant diffusion, high junction leakage, EOT scaling, Dit reduction and enormous dislocation defects in the Ge epi-layer on Si substrates because of the large lattice mismatch to Si. Herein, we propose a feasible pathway to scale the Ge MOSFET technology by using a novel diamond-shaped Ge gate-all-around (GAA) nanowire (NW) FETs.

In addition, a high-quality, fine-controlled, atomic-thin interfacial layer (IL) between the Ge channel and high-k gate dielectric is crucial for EOT scaling and device performance, but remain challenging because of the unstable IL of germanium oxide and decomposition of several germanium suboxides (GeyOx) [1], [2]. The damages induced by fin dry etching on the three-dimensional (3D) sidewalls was also reported to degrade the interface quality [3]. In this paper, an effective interface engineering technique, in-situ ALD O_3 treatment, is proposed to treat the Ge channel surface in a standard atomic layer deposition (ALD) chamber prior to high-k dielectric deposition. In-situ ALD O_3 treatment effectively removes the Ge surface damages and roughness that arise from anisotropic dry etching of nanoscale fins by using precisely controlled layer-by-layer oxidation followed by desorption of GeO, as shown in Fig. 1.

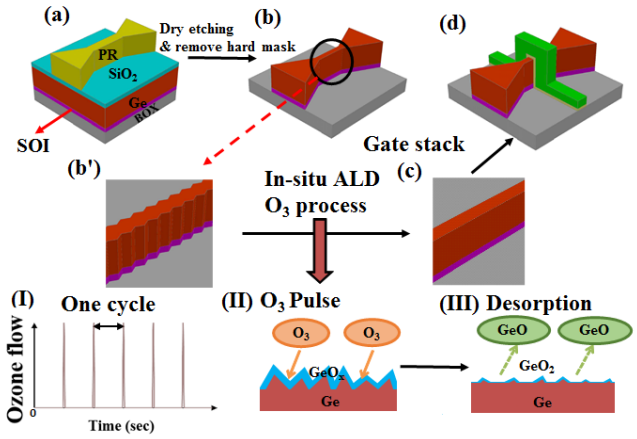

Fig. 1

References:

[1] Sheng Kai Wang et al., J. Appl. Phys., p. 054104.
[2] A. Toriumi et al., IEDM 2011, p. 646.
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