High quality UTB GeOI by HEtero-Layer-Lift-Off (HELLO) technology for future Ge CMOS application

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1. Introduction

Ultrathin body (UTB) Ge-on-insulator (GeOI) is compulsory structure for improved gate control and immunity against short channel effects in the ultimately scaled high performance and low power CMOS. However, severe carrier mobility degradation has been reported in commercially available Smart-Cut^{TM} GeOI substrates with body thickness (T_{body}) less than 20 nm.[1,2] Unstable Ge/buried oxide (BOX) interfaces, poor Ge crystallinity and Ge thickness fluctuation in UTB GeOI are main challenges for feasible Ge CMOS application. Therefore, more sophisticated fabrication methods of UTB GeOI are strongly required. In this work, a novel Ge layer transfer technology called HEtero-Layer-Lift-Off (HELLO)[3] utilizing SiGe etch stop layer and Si passivation layer has been developed for precise control of T_{body} and back interfacial quality in UTB GeOI. Enhancement of carrier mobility in UTB GeOI *n*/*p*MOSFETs has been demonstrated, showing high potential of UTB GeOI by HELLO technology.

2. Experimental procedures

UTB GeOI substrates were prepared through HEtero-Layer-Lift-Off (HELLO) technique (Fig. 1). As a donor structure, Ge channel/$Si_{0.3}Ge_{0.7}$ etch stop layer/Ge buffer layer/AlAs/GaAs hetero-structures were grown by low-pressure CVD. To improve back interfacial quality, Si passivation layer on top of Ge layer prior to ALD-Al_2O_3 deposition were carried out especially for *p*MOSFETs. Then, the direct bonding to SiO_2/Si host substrate was performed in press machine under vacuum at 200 °C. Note that the direct bonding was performed at interface of Al_2O_3/SiO_2 to prevent the damage for Ge channel layer. To release GaAs substrate, the AlAs layer was etched selectively and laterally in HCl solution at room temperature. Then, the Ge buffer layer and $Si_{0.3}Ge_{0.7}$ etch stop layer were etched, sequentially. This HELLO technology was performed at low temperature to avoid thermal stress, leading to high quality GeOI structure.

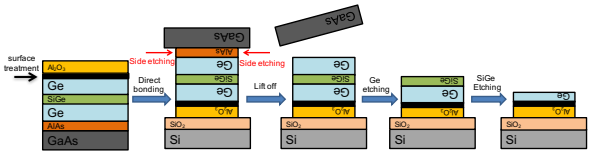

Fig. 1 Schematic flows of Hetero-Layer-Lift-Off (HELLO) technology for fabricating UTB GeOI substrates.

3. Results and discussions

The XTEM of ultrathin GeOI channel (3 nm) in MOSFETs fabricated through HELLO technology is shown in Fig. 2. Single crystalline Ge layer with precise channel thickness control down to 3 nm was achieved.

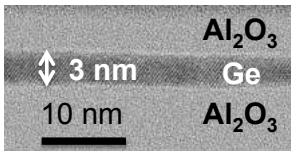

Fig. 2 XTEM of ultrathin GeOI channel fabricated with HELLO technology.

Fig. 3(a) shows the thickness dependence of effective hole mobility at N_s of 5×10^{12} cm^{-2} in UTB GeOI *p*MOSFETs.[4] The devices fabricated with HELLO technology exhibited much higher mobility of about 200 cm^2/Vs in the UTB regime. The trend of mobility degradation with scaling T_{body} was also suppressed for the devices fabricated with HELLO technology, presenting the clear benefit of reducing thickness fluctuation and Si-passivated back interface. On the other hand, the thickness dependence of effective electron mobility in UTB *n*MOSFETs was shown in Fig. 3(b).[5] It was confirmed the effective electron mobility significantly increased with scaling T_{body} below 10 nm, which may be attributed to suppression of Ge thickness fluctuation and modulation of Ge conduction band structure.

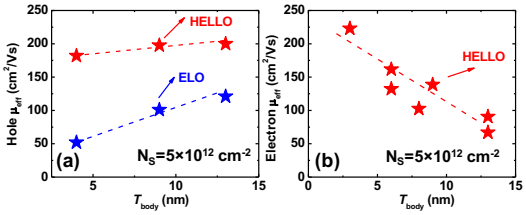

Fig. 3 (a) T_{body} dependence of effective hole mobility at N_S of 5×10^{12} cm^{-2}, (b) T_{body} dependence of effective electron mobility at N_S of 5×10^{12} cm^{-2}.

4. Conclusion

High quality GeOI substrates have been successfully fabricated through HELLO technology. Both electron and hole mobility enhancement were confirmed, indicating UTB-GeOI is very promising for future Ge CMOS applications.

References

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