Enabling Improved Contact Resistivity for Si, Ge and GeSn Technology

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Si-based FinFET is the main technology that fuels the advanced nanoelectronic circuits. As FinFETs aggressively shrink, parasitic resistance dominated by contact resistance at the interface of contact metal becomes one of the critical challenges in achieving high performance due to the ever smaller contact area. When the technology enters Ge or GeSn regime for higher performance, the issue is more challenging because of the pronounced Fermi level pinning (FLP) effect due to smaller bandgap and higher dielectric constant than Si, making it difficult to modulate Schottky barrier height (Φ_B). This talk will briefly discuss the progress of contact technology for Si-, Ge- and GeSn-based process platform. For Si-based platform, Ge pre-amorphization implantation (PAI) prior to contact silicide formation with reverse retrograde profile or at cryogenic temperature were explored. N-FinFETs demonstrate higher drive current by 12 % for the former process due to decreased series resistance and significantly improved variation in device parameters such as sub-V_t swing (SS), drain induced barrier lowering (DIBL) and total series resistance by 22 %-34 % for the latter process due to end of range (EOR) defects. For Ge-based platform, Ti germanide including C54 phase on P-implanted Ge is found to be effective to alleviate FLP. With additional P implantation after Ti germanide, further improved contact resistivity by a factor of 4.2 is obtained which is ascribed to the enhanced dopant segregation at the germanide/Ge interface. For GeSn-based plat form, O_2 plasma treatment prior to contact metal deposition or formation of Yb stanogermanide ($Yb_3(Ge_{1-x}Sn_x)_5$) on GeSn were proposed to improve contact resistance by Fermi level depinning due to suppressed surface states. The significant Fermi level depinning is evidenced by the Φ_B of 0.12~0.13 eV with contact resistivity less than 4.0×10^{-7} Ω-cm^2. The newly developed contact processes are fully compatible with the incumbent VLSI technology and gain an outlook on empowering high-performance Ge and GeSn devices.