Evolutional OPC as DTCO :
OPC Shot Counts Optimization on SPT Mask Technology

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In response to the ultra-miniaturization needs of semiconductors, the lithography mask technology in the sub 20 nm node is demanding more sophistication and evolution in advanced exposure technologies such as immersion exposure, inverse lithography and multi-beam mask writing has been done.

In particular, by co-optimizing the layout design method and the OPC (Proximity Effect Correction) method as DTCO (Design Technology Co-Optimization), it is essential to realize a pattern that is close to the design layout as much as possible, and to expand the device performance and the process margin.

Among others, extremely high precision technology is required from the viewpoint of accuracy, defects, cost, etc., for a mask making technology for transferring and exposing a design layout onto a wafer substrate. As the densification needs of the target VLSI design pattern rapidly increases, the application of the OPC (Proximity Effect Correction) method, optimization development and manufacture has become indispensable.

In this paper, when implementing the 16 nm node generation with the most general-purpose needs as one layer mask immersion lithography (SPT: Single Pattern Technology), mask data to be made larger and more complicated, and a longer drawing time of mask layout design guidelines to deal with the problem were studied by computer simulation (Tachyon ™) and mask drawing experiment.

According to the previous research by the authors and the like, it has been found that optimization setting of OPC is most complicated (single-layer mask exposure method (SPT)) (data capacity increase) and mask drawing time is prolonged. In contrast, as the two-layer divided mask exposure system (DPT) and the four-layer divided mask exposure system (QPT) are used, the OPC optimization setting tends to reduce the data capacity and mask writing time. That is, QPT <DPT <SPT.

SPT is more advantageous than the other two methods from the standpoint of productivity and cost of exposure, while multi-masking becomes disadvantageous in the order of SP> DPT> QPT. However, in order to expose a VLSI layout design on a wafer substrate with high resolution and high accuracy, SPT needs to estimate its application limit and design accuracy sufficiently and establish optimal conditions. According to the previous research by the authors and others, it has been found that in the case of an SRAM having six Fin transistors of 16 nm node, the resolution limit is about 80 nm between the gates.

In this research, we focused on this SPT study case, and further detailed OPC optimization was carried out by computer lithography to obtain the optimum shot count by Mask Rule Check (MRC). Based on this, a mask was actually created by electron beam exposure, CD and shape of the resist pattern on the mask substrate were measured with CD-SEM and verified.

The conclusion is that for the 16 nm node Fin Tr type SRAM gate layer, the minimum OPC space is 10 nm to 15 nm (Fig.1). It became clear that the mask drawing shot count is reduced and the drawing time is minimized. Moreover, it was confirmed that this condition can be effectively used in pattern analysis by actual mask drawing experiment from the viewpoint of pattern shape, CD etc. (Fig.2).　As a result, the prospect of realizing the ultimate SPT method was obtained.

These results were able to verify the possibility of device performance prediction (I-V, SNM, etc.) References by conventional TCAD from the viewpoint of mask experiment.

References:
K.Kadota et al., IEICE-1985, SPIE-922 (1988), SPIE-1088 (1989), PMJ-2011, PMJ-2013, PMJ-2016, MNC-2011, JSAP-2016, JSAP-2017, NGL-2017
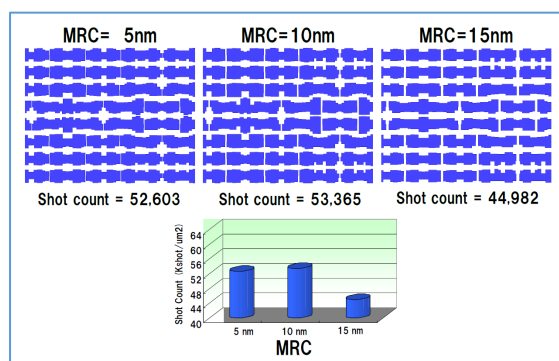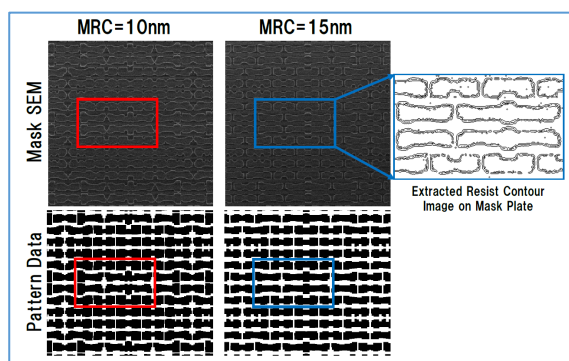
Fig.1 Example of Shot Count vs MRC

Fig.2 Example of Mask SEM Image vs MRC