Catalyst-free formation and hole gas accumulation in core-shell and core-double shell

nanowires using Si and Ge

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Abstract:

One dimensional nanostructures, such as silicon (Si) and germanium (Ge) nanowires, (NWs) have been suggested as building blocks of vertical type metal oxide semiconductor field effect transistors (MOSFETs) with high speed and low energy consumption [1-2]. The general method to the synthesis of the NWs is chemical vapor deposition (CVD) approach based on the vapor-liquid-solid (VLS) growth mechanism that requires metal as catalysts, such as gold, which causes contamination in the NW structure and affects their properties. Development of catalyst-free growth of NWs becomes more important for NW research. In this study, we showed the feasibility of using catalyst-free method to fabricate p-Si/i-Ge coreshell NWs and p-Si/i-Ge/p-Si core-double shell NWs with well-ordered heterojunction structures. Before shell formation, a precise diameter control for the Si core NWs was realized by a simple thermal oxidation process, showing the prevention of metal catalyst contamination, as shown in Fig.1. The hole gas accumulation could be reliably detected from i-Ge shell region in p-Si/i-Ge core-shell NW and p-Si/i-Ge/p-Si core-double shell NW arrays, which were evaluated by a peak shift and asymmetric broadening of Ge optical phonon peaks. Transmission electron microscopy (TEM) with energy dispersive x-ray (EDX) mapping showed good crystallinity and sharp interface as shown in Fig. 2. These results indicated that carrier transport region could be separated from the impurity doped region and therefore suppressed impurity scattering by constructing core-shell structures.



Figure 1. (a) non-treated (b) thermal oxidation method. Scale bar is 1 um.



Figure 2. EDX mapping (a) p-Si/i-Ge/p-Si NWs, (b) Ge optical phonon peask observed for bulk Ge, p-Si/i-Ge core-shell, p-Si/i-Ge/p-Si core-double shell NWs.

References:

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