Demonstration of HfO_2 based Ferroelectric FET with Ultrathin-body IGZO for High-Density Memory Application

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Recently, ferroelectric HfO_2 FET memories have attracted more attentions[1], because of its good CMOS compatibility non-destructive readout, low power consumption and high program/erase speed. High density 3D vertical structure FeFET with poly-Si channel has been proposed and demonstrated, successfully[2]. However, vertical FeFET has some challenges, including low mobility of very thin poly-Si channel, V_{th} compensation and degraded subthreshold slope (SS) by charge trapping, and voltage loss by low-k interfacial layer on Si channel. IGZO is a promising channel material for vertical 3D structure memories, thanks to high mobility of very thin channel[3][4], less charge trapping and voltage loss by nearly-zero interfacial layer at low thermal budget.

In this paper, a junctionless FeFET with very thin IGZO channel and $HfZrO_2$ (HZO) is proposed to overcome the problems of poly-Si channel. We design and fabricate the device and demonstrate its potential as a lower power, high density memory device.

Design and experimental results

Bottom gate IGZO FeFET was simulated for exploring the design space. Fig.1 shows the simulation result of junctionless IGZO FeFET with conventional bottom gate TFT structure. The memory window does not exist. Due to the junctionless structure and floating body, the voltage across HZO layer is very small and polarization is difficult to switch. In order to increase the voltage across HZO layer, the body potential is fixed by top gate. The memory window exists with top gate because larger electric field can be effectively applied to FE-HfO_2 layer especially as shown in Fig. 2.

We fabricated the bottom gate IGZO FeFET for the proof-of-concept as shown in Fig. 3. As top gate oxide SiO_2 become thinner, memory window becomes larger. 12 nm SiO_2 is chosen to suppress leak current. For vertical 3D structure, the channel should be sufficiently thin8 nm-thick IGZO is chosen because of high Vth, low SS.Fig. 4 shows the cross sectional TEM image of a fabricated device. Each layer is uniformly formed. HZO and IGZO channel are free of low-k interfacial layer. The field-effect mobility is extracted from I_d-V_g curve and is shown in Fig. 5. There is no significant mobility degradation with HZO compared to SiO_2. The mobility of IGZO channel can be higher than poly-Si with same body thickness. Fig. 6 shows the measured I_d-V_g curve of IGZO FeFET. The 0.5 V memory window exists with almost ideal SS of 60mV/dec. IGZO FeFET shows potential for low-power and high-density application.

Reference: [1] J. Muller et al., VLSI Symp. 2012 [2] K. Florent, et al, IEDM 2018. [3] K. Nomura et al., Nature, 2004. [4] T. Kawamura et al., IEDM 2008.

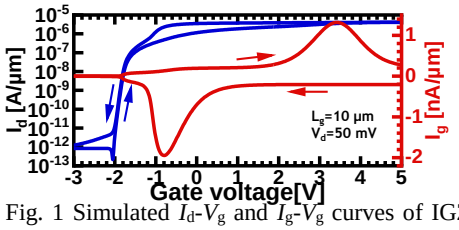

Fig. 1 Simulated I_d-V_g and I_g-V_g curves of IGZO FeFET for floating body. MW do not exist.

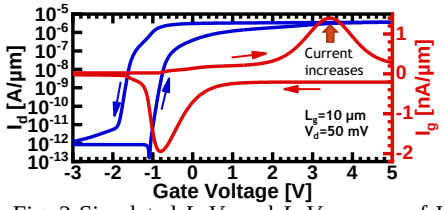

Fig. 2 Simulated I_d-V_g and I_g-V_g curves of IGZO FeFET for fixed body potential. MW exists.

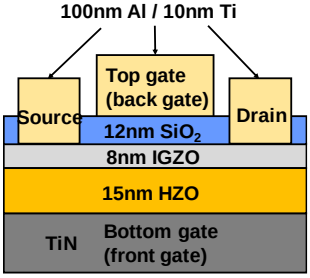

Fig.3 bottom gate with optional top gate structure of IGZO FeFET.

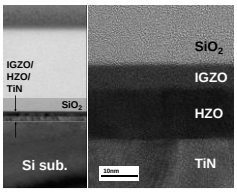

Fig. 4 TEM image of TiN/HZO/IGZO/SiO2 stack. IL is nearly zero.

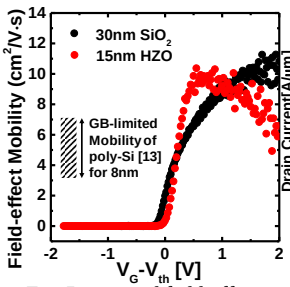

Fig. 5 extracted field-effect mobility of IGZO channel. Hall mobility is 10cm^2/V·s.

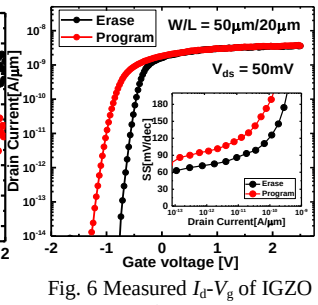

Fig. 6 Measured I_d-V_g of IGZO FeFET after Erase / Program. MW ~0.5V appears.