Improved subthreshold characteristics of p-type poly-Si junctionless transistor by utilizing optimized channel structure

Min-Ju Ahn, Takuya Saraya, Masaharu Kobayashi, and Toshiro Hiramoto
Institute of Industrial Science, University of Tokyo
E-mail: mjahn@nano.iis.u-tokyo.ac.jp

[Introduction] A junctionless (JL) transistor requires thin channel for full depletion in turn-off state [1]. However, total series resistance increases as the channel thickness becomes thinner. In this regard, the trench (or elevated S/D) structure can be a solution to cope with this problem [2, 3]. The trench structure has two different regions: (1) thin channel region for full depletion in turn-off state, (2) thick S/D regions for high drain current (I_D) in turn-on state. Hence, subthreshold characteristics are mainly determined by this thin channel region. However, there are few studies reported on how it affects the subthreshold characteristics. In this work, we proposed a p-type poly-Si JL transistor with optimized channel structure which has self-aligned low doped thin region and heavily doped thick region. It exhibits excellent electrical performances such as average steep subthreshold slope (SS) of 84mV/dec and high on/off current ratio of $1.4x10^8$ without any hysteresis, which are better than those of previously reported planar-type poly-Si JL transistors [2-4].

[Experimental] Fig.1 shows the main process flows of fabricated JL transistor. BF_2^+ ions were implanted into 80nm-thick SPC poly-Si film at 35keV with dose of $3x10^{14}cm^{-2}$ for p-type channel (a). Subsequently, the channel active region was locally thinned down to 15nm by oxidation, while the S/D regions remained thick to form the trench structure (b-c). Here, the concentration of boron is reduced after oxidation due to the out-diffusion and segregation effect of boron atoms. By using this effect, the locally low doped thin region can be automatically obtained (d). After that, a 10nm-thick dry oxide was thermally grown as a gate oxide. The final channel thickness of thin region is 10nm. Then, a 150nm-thick in-situ doped n^+poly-Si was deposited for a gate electrode (e). The channel width (W_{ch}), length (L_{ch}) and thickness (T_{ch}) are 10μm, 30μm and 10 nm, respectively.

[Results and Discussion] Fig.2 shows the I_D-V_G curves of fabricated JL transistors at V_D=-0.05 and -1.2V. Apparently, steep SS, high on/off current ratio and low I_{off} are observed without hysteresis, while maintaining reasonable on current. Fig. 3 shows I_D-V_D curves. Fig. 4 shows SS extracted in subthreshold region at V_D=-0.05 and -1.2V. It can be clearly seen that the steep SS (SS_{min}=78mV/dec at V_D=-0.05V, 63mV/dec at V_D=-1.2V, SS_{ave}=95mV/dec at V_D=-0.05V, 84mV/dec at V_D=-1.2V) values are observed even in planar-type device with large dimension. Typically, the steep SS of poly-Si transistors could be obtained in multi-gate structures by scaling the channel dimension as well as T_{ch} because it reduces the total number of traps inside poly-Si channel. Besides, the locally low doped thin region can make the SS steeper by reducing depletion width in partially depleted region.

[Conclusion] The proposed concept is very helpful for improving the subthreshold characteristics of JL transistor. In addition, it can be expected the subthreshold characteristics are more enhanced by applying multi-gate configurations. Therefore, it is likely to be useful in three-dimensional (3-D) stacked applications.

[Reference] [1] J. -P. Colinge *et al*., Nature, vol. 5, p. 225, 2010. [2] H. B. Chen *et al*., IEEE Electron Device Letters, vol. 34, p. 897-9, 2013. [3] Y. B. Liu *et al*., SNW, p. 1-2, 2015. [4] H. C. Lin *et al*., IEEE Electron Device Letters, vol. 33, p. 53-5, 2011.

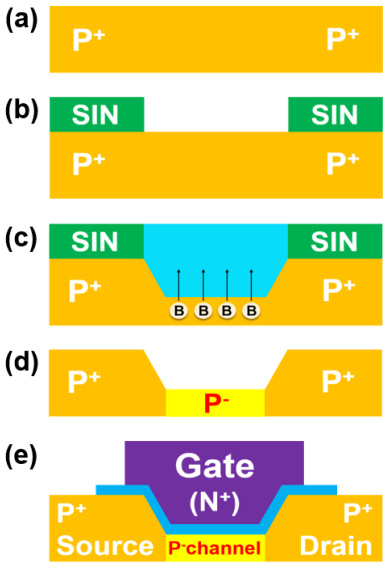

Fig.1: Fabrication process flows.

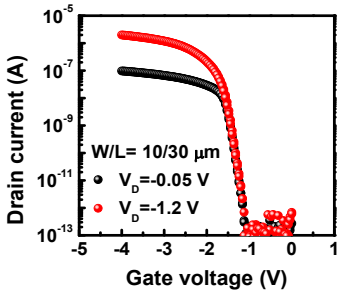

Fig.2: I_D-V_G characteristics.

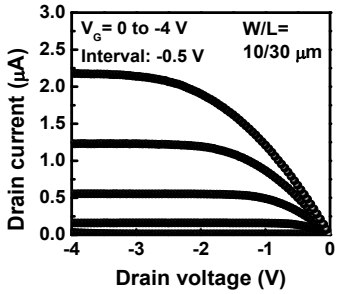

Fig.3: I_D-V_D characteristics.

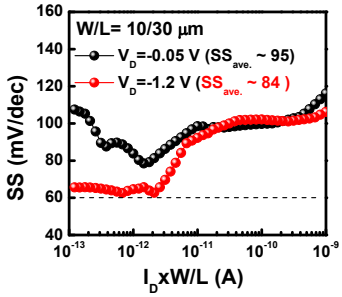

Fig.4: Extracted SS values in subthreshold region.