Fabrication of closely packed magnetic arrays for physical reservoir computing

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Reservoir computing has been demonstrated in several physical reservoirs such as optical laser[1)], soft materials[2)] and spintronics devices[3, 4)]. These physical reservoirs have functions of nonlinear transformation and fading memory. The functionality can be realized by complex magnetization dynamics in closely packed magnetic dot array. It has been simulated that a reservoir consisting of a dipole-coupled magnetic dot array can perform binary logic functions of AND, OR and XOR[5)]. In the magnetic reservoir, gap between neighboring dots was as small as 20 nm, which causes sufficient magnetic coupling between the dots. Such a small gap, however, is difficult to make by means of conventional fabrication process. Also, electrical contacts to individual dots are also necessary to read out magnetization states.

In this study, we investigate experimentally the magnetic physical reservoir using closely packed magnetic tunnel junction (MTJ) array. The MTJs makes it possible to read the magnetization states through magnetoresistance effect. Previously we reported that 8x8 MTJ dot arrays were fabricated using electron beam (EB) lithography, ion etching, and lift-off technique[6)]. MTJ film had a stack of buffer layer/Co-Pt based fixed layer/MgO/CoFeB free layer/MgO cap layer/metal cap layer. The smallest gap was about 20 nm, which corresponds to the simulation model[5)]. Although fundamental fabrication process was developed, there were some issues remained. Using the process, in some arrays it was difficult to align precisely the positions of the MTJ dot, contact hole and point of top lead. Another issue was breaking of Cu top lead patterns, which was as thin as 30 nm. The breaking of the top lead was observed at rough edges of the bottom electrode (several 100 nm in step height). As a result, process yield was not high in the previous fabrication process.

In this report, we improved the fabrication procedures for the EB alignment and top lead. For the EB alignment, we changed the design of the chip marks beside the dot array, which consisted of a set of cross shaped patterns. Consequently, the variation of the chip mark width was suppressed, resulted in the enhancement of the yield of the alignment. To avoid the breaking of the top lead, we made the thin top leads as short as possible. Instead a thick Cr/Au electrode patterns were extended inward to step over the rough edges. We observed that the short Cu lead patterns were properly fabricated. This research and development work was partly supported by the Ministry of Internal Affairs and Communications.

1) L. Appeltant,et al.: Nat Commun. 2 (2011)468. 2) K. Nakajima, et al.: Sci Rep. 5 (2015)10487. 3) J. Torrejon, et al.: Nat. 547 (2017)428. 4) R. Nakane, et al.: IEEE Access. 6 (2018)4462. 5) H. Nomura, et al.: Jpn. J. Appl. Phys. 58 (2019)070901. 6) H. Kubota, et al., JSAP 2019 Spring Meeting, 9p-PB1-74.