The effect of Hf-ion implantation on the charge trapping characteristics of MONOS-type memory devices

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Introduction: The Metal-Oxide-Nitride-Oxide-Semiconductor (MONOS)-type memories have received significant attention in embedded non-volatile memory (NVM) applications. Electrons or holes are injected into the silicon nitride film from the silicon substrate via a tunnel oxide film following the quantum tunneling mechanism [1]. The injected charge carriers then get captured by trap centers in the nitride film. The limited number of trap centers in the nitride film is a crucial problem in the performance enhancement of MONOS-type memories [2]. In this work, the effect of Hf-ion implantation into the nitride film on the memory performance has been studied.

Experimental Setup: A thin tunnel oxide film of 2.4 nm in thickness was grown by rapid thermal oxidation (1050 ℃) of p-type (100) silicon substrate. A 30.4-nm-thick silicon nitride film was formed at 600 ℃ by low-pressure chemical vapor deposition (LPCVD) using Si_2Cl_6 and NH_3 gases. A thick blocking oxide film (17.3 nm) was deposited at 400 ℃ using a PECVD technique. The silicon nitride film was implanted with hafnium ions of 3 x 10^{13} cm^{-2} at 55 keV. Finally, an aluminum gate electrode was deposited by a vacuum evaporation method to form memory capacitors.

Results and Discussion: Figures 1 and 2 show the flat-band voltage shift (ΔV_{FB}) at different programming and erasing voltages, respectively. The capacitors with Hf-ion implantation followed by annealing at 800 ℃ provide relatively larger ΔV_{FB} values for programming voltages, while a slight difference is observed between the non-implanted and Hf-ion implanted capacitors with annealing at 600 ℃. On the other hand, in the erasing operation, the Hf-ion implanted capacitors with annealing at 600 ℃ provide smaller ΔV_{FB} values compared to the non-implanted capacitors, as shown in Fig. 2. The Hf-ion implanted capacitors with annealing at 800 ℃ show comparatively small ΔV_{FB} values. Further results in terms of electron spin resonance (ESR) and the charge retention characteristics will be discussed in the presentation.

References: [1] E. Suzuki, H. Hiraishi, K. Ishii, Y. Hayashi, *IEEE Trans. Electron Devices*, **30**, 122 (1983). [2] S. R. A. Ahmed, K. Kato, and K. Kobayashi, Mater. Sci. Semicond. Process. 70 (2017) 265-271.

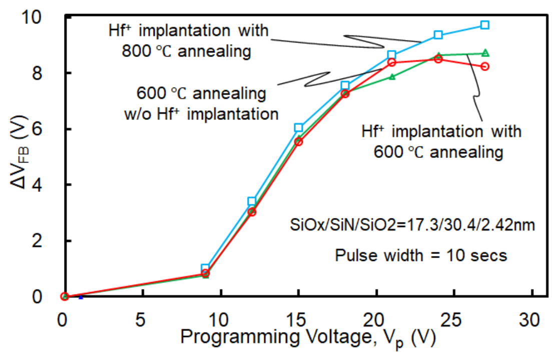

Fig. 1. ΔV_{FB} at different programming voltages.

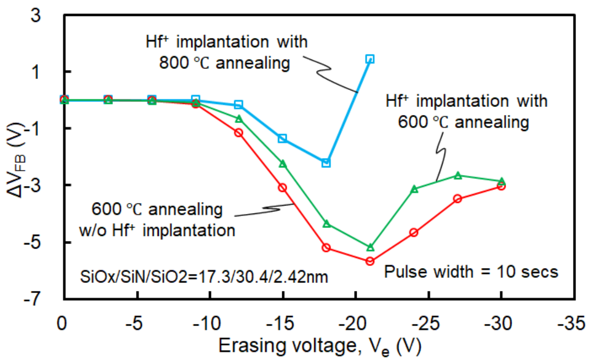

Fig. 2. ΔV_{FB} at different erasing voltages.

Acknowledgment: I want to express my gratitude to H. Mino, K. Niisato, Y. Sanbongi, T. Umezawa, S. Matsumoto, S. Matsudaira, and Y. Kayamori for their valuable discussions. I want to express my gratitude to T. Kuroi from Nissin Ion Equipment Co., LTD. This work was partly supported by a Grant-in-Aid for Scientific Research (No. 26420280) from JSPS.