Experimental demonstration of n- and p-channel GaN MOSFETs operation for power IC

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Introduction

A GaN power integrated circuit (IC) consisting of GaN logic circuits is a promising candidate for a future power IC with a low power consumption and high performances. In order to realize the GaN power IC, n- and p-channel MOSFETs with high performances are mandatory. In this study, in order to demonstrate n- and p-channel GaN MOSFETs' operations with the same gate stack structure, the inversion mode n-channel and accumulation mode p-channel GaN MOSFETs are fabricated and evaluated.

Experimental, results and discussion

The fabricated device structures are shown in Fig. 1. Figure 2 (a) shows the drain current (Id)–gate voltage (Vg) transfer characteristics obtained at drain voltage of 50 mV of GaN-MOSFETs (L/W=100/100μm) fabricated under various PDA conditions. The n-channel GaN-MOSFETs have the normally-off operation characteristics with threshold voltages of approximately 1.5 V. All fabricated devices perform clear I_{on}/I_{off} ratio characteristics with low gate leakage currents of the order of 10^{-15}A/μm. Impressively, well-behaved I_{on}/I_{off} state (~10^4) and leakage current (< 10^{-16} A/μm) have been also observed in the p- channel GaN-MOSFETs. The superior result obtained in this work has proved the possibility of the fabrication of the p-channel MOSFET without the necessity of two-dimension hole gas (2DHG) sources of heterostructures, which has not been certificated to date. Moreover, it is shown that the n-channel and p-channel MOSFETs annealed at 700°C perform the highest on-state currents. The effective electron/hole channel mobility characteristics of fabricated devices are calculated using the I_d–V_g and C-V characteristics, as shown in Fig. 2(c). The gate voltages where the field effect electron mobilities reach the highest values correspond to the carrier concentration (N_s) region from ~10^{12} to 10^{13}cm^{-2}. The peaks of electron mobility are 70, 75, and 105 cm^2 V^{-1} s^{-1} in devices untreated with PDA process and annealed at 500°C, 700°C, respectively. The similar effect of the PDA treatment of PEALD-Al_2O_3 on p-channel MOSFETs has been confirmed again. While the I_{on}/I_{off} states are unclear and almost unobservable in samples consisting of dielectric films untreated with PDA and annealed at 500°C, respectively, the sample annealed at 700°C performs a good pinch off characteristic (~10^4). For the first time, the field effect hole mobility of approximately 0.2 cm^2/V·s is measured in the p-channel GaN-MOSFETs at room temperature, as shown in Fig. 2 (c). The channel electron and hole mobility obtained in GaN-MOSFETs are lower than those of bulk's materials. Matthiessen's rule has identified many mechanisms determining the channel mobility, such as bulk mobility, Coulomb scattering mobility, surface phonon mobility, etc. It can be concluded that the low channel mobility is more attributed by GaN crystallinity, and/or coexistence of carriers originated from defect states than oxide and/or interface trapped states.

The world's first depletion-mode p-channel GaN MOSFETs fabricated in this work is a proof that high-performance p-channel GaN-MOSFETs are obtainable if further improvement of the p-GaN deposition by reducing the structural defects in epilayers and optimizing the device processing can be solved. Therefore, the idea of the fabrication of GaN power IC may be realized.

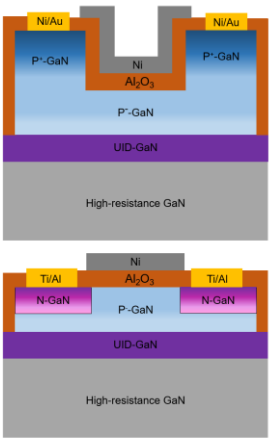

Figure 1. Cross-sectional views of n- and p-channel GaN MOSFETs

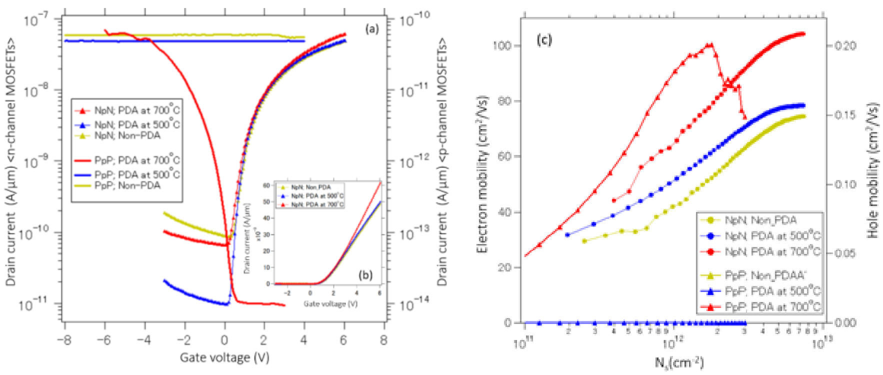

Figure 2. Id–Vg characteristics in logarithmic scale (a), linear scale (b) and electron/hole mobility of n and p-channel GaN-MOSFETs (c)