Effect of annealing temperatures on surface passivation quality of Cat-CVD p-a-Si on c-Si

Huynh Thi Cam Tu, 大平　圭介, 松村　英樹

JAIST

E-mail: tu-huynh@jaist.ac.jp

Crystalline silicon (c-Si) solar cells using interdigitated back contact amorphous-silicon (a-Si)/c-Si heterojunction (IBC-SHJ) structures are very promising to obtain high conversion efficiency. However, the fabrication of IBC-SHJ cells is considered complex, particularly for the back-side contact formation process. To further reduce manufacturing costs and lower the price of the solar cell, a decrease in the number of cell fabrication process steps is required. For this purpose, we have developed a simple process for fabricating back-electrodes of the IBC-SHJ cells. In this process, PH_3 ions are implanted into Cat-CVD p-type a-Si (p-a-Si) to convert conduction type of some desired patterned areas to n-type. An annealing is required to remove the defects, and then, to restore passivation quality of the a-Si [1]. The p-a-Si layers are also affected by this annealing process. There is a significant shortage of knowledge about influence of thermal treatment on passivation quality of the Cat-CVD a-Si layers, although the PECVD p-a-Si was reported to have poor thermal resistance [2]. Therefore, in this presentation we report a detailed study of the effect of annealing temperature on surface passivation quality of Cat-CVD p-a-Si on c-Si.

Surface passivation quality of p-a-Si was evaluated by measuring effective minority carrier lifetime (τ_{eff}) of p-a-Si/intrinsic a-Si (i-a-Si)/c-Si/i-a-Si/p-a-Si structures by microwave photo conductive decay method (μ-PCD). Figure 1(a) shows τ_{eff} of c-Si with p-a-Si layers formed by Cat-CVD at substrate temperatures (T_{sub}) from 100 to 300 °C, and by PECVD at a T_{sub} of 155 °C [2] as a function of annealing temperature. This figure clearly shows that Cat-CVD p-a-Si films have rather low thermal resistance which is similar to the PECVD counterpart. Passivation quality of p-a-Si films was degraded by annealing at 225–250 °C, which is considered to be due to the effusion of hydrogen (H) atoms. Therefore, annealing temperature applied to ion implanted p-a-Si is limited at about 250 °C [1]. In addition, we have confirmed that H effusion can be reduced by forming a Cat-CVD Si nitride (SiN_x) cap layer on surface of p-a-Si. Figure 1(b) shows τ_{eff} of the samples with and without SiN_x cap layer after annealing at 350 °C as a function of SiN_x thickness. Note that the SiN_x was completely removed before measuring τ_{eff}. It can be seen that p-a-Si with a good passivation quality can be attained even after annealing at a temperature as high as 350 °C by using a SiN_x cap layer to deduce H effusion.

This work is financially supported by NEDO project, Japan.

[1] H.T.C.Tu et al., Thin Solid Films 683 (2019) 150.
[2] S. D. Wolf et al., J. Appl. Phys. 105 (2016) 103707.

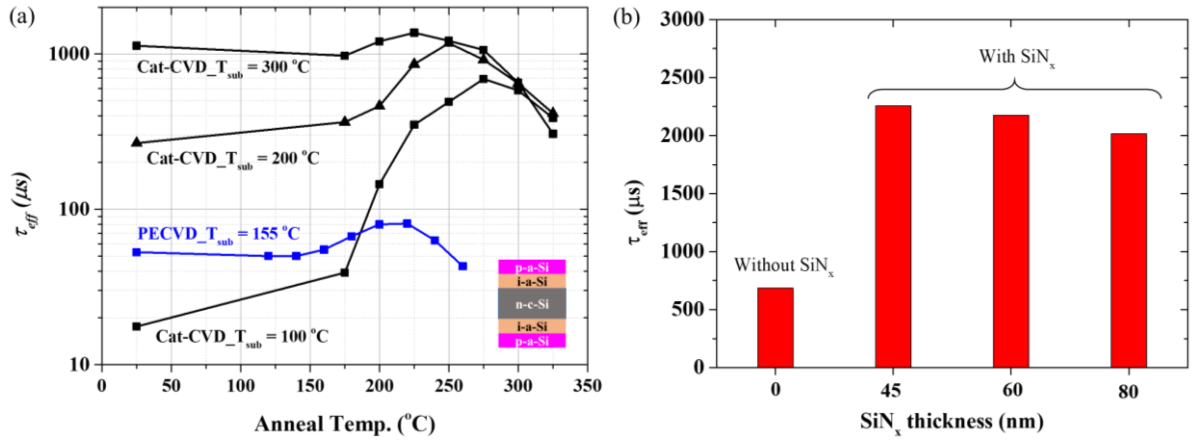

Figure 1: (a) τ_{eff} of c-Si with Cat-CVD and PECVD p-a-Si films as a function of annealing temperature, (b) τ_{eff} of c-Si with Cat-CVD p-a-Si with and without SiN_x capping layer after annealing at 350 °C for 30 min (SiN_x was completely removed before measuring τ_{eff})