Effect of annealing temperature on Al_2O_3/NAOS/Si MOS interface properties

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Aluminum oxide (Al_2O_3) and Silicon nitride (a-SiN_x:H) provide an outstanding level of interface passivation on crystalline silicon. An ultrathin SiO_2 layer formed by nitric acid oxidation of Si (NAOS) was used in combination with SiN_x to improve the interfacial properties of Si solar cells [1]. In order to understand the passivation properties of Al_2O_3/NAOS combination layer, in this work, we investigated the influence of post-annealing temperature on the interfacial properties at the Al_2O_3/NAOS/Si MOS structure.

A p-type Si (100) wafer with 8~10 Ω cm resistivity was cleaned using the RCA method, followed by etching with a 5 % hydrofluoric acid (HF) solution to remove the chemical oxide layer. Then, the wafer was immersed in 61wt% HNO_3 solutions at 80 ℃ for 30 min. The thickness of NAOS SiO_2 layer was estimated to be 1-1.5nm by ellipsometry. Next, 50nm-thick film of Al_2O_3 was grown by thermal atomic layer deposition (ALD) at temperature of 300 ℃ on the both sides of the Si substrate with the NAOS layer. After being coated with Al_2O_3, the samples were annealed at 450, 500, and 650 ℃ for 30 min in a N_2 atmosphere. Minority carrier lifetime measurements were obtained by Quasi-Steady-State Photoconductance (QSSPC). The capacitance-voltage (*C-V*) measurements were carried out to characterize the contributions of field-effect and chemical passivation of the NAOS/Al_2O_3 films.

Figure 1 shows the measured carrier lifetimes of Si/NAOS/Al_2O_3 films annealed at various temperatures. After annealing at 450 ℃, the carrier lifetime greatly increases to 140 μs, however, for annealing temperature higher than 500 ℃, the minority carrier lifetime decreases sharply with increasing of temperature. According to *C-V* measurements, we found out that the samples with the highest lifetime do not correspond to the high fixed charge density. In addition, the interface state density (D_{it}) values as a function of energy position are shown in Fig. 2. It is clear that annealing at higher temperatures resulted in higher D_{it} values at deep energy levels, whereas for the case without NAOS layer, D_{it} values decreases with increasing annealing temperature 450-600 ℃[2]. Although the reaction between Al and SiO_2 due to post-annealing can lead to a change of slow states density and oxide fixed charges [3], further investigations have to be performed to inspect the function of these layers on a microscopic scale.

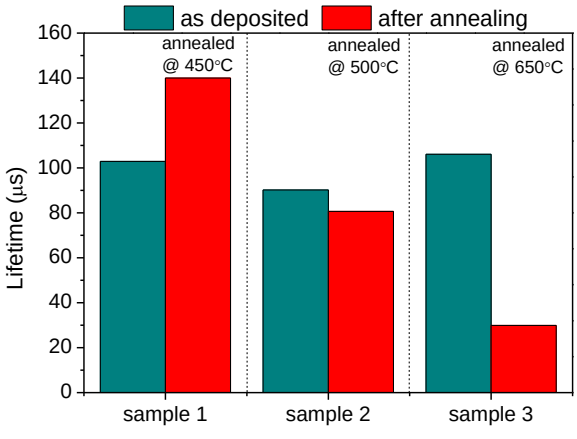

Fig. 1 Comparison of minority carrier lifetime of <Al_2O_3/NAOS/Si/Al_2O_3> structure without and with annealing treatment performed at 450, 500, and 650℃.

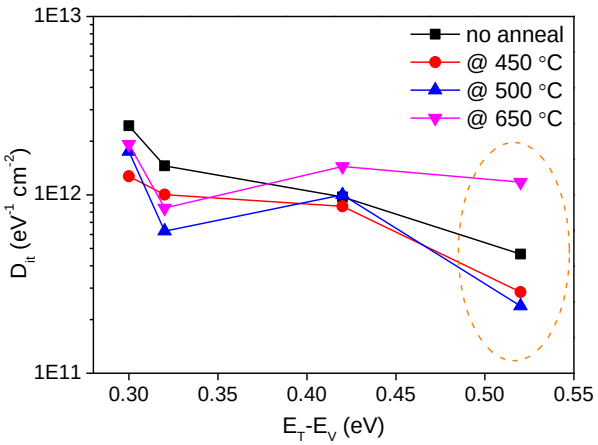

Fig 2 Interface state density D_{it} as a function of energy position in the silicon bandgap

[1] Mihailetchi, Valentin D., Yuji Komatsu, and L. J. Geerligs. Applied Physics Letters 92.6 (2008): 063510.
[2] Kersten, Friederike, et al. Energy Procedia 38 (2013): 843-848.
[3] Yanase, et al. Electrochemical and Solid-State Letters 13.7 (2010): H253-H256.