Toward high modulation efficiency of III-V/Si hybrid MOS optical phase shifter by equivalent oxide thickness scaling

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【Introduction】 A high modulation efficiency is desirable for both optical modulators and optical switches which are fundamental building blocks for optical interconnection systems. By integrating III-V materials on a Si waveguide to form a III-V/Si hybrid metal-oxide-semiconductor (MOS) capacitor via wafer-bonding technology, efficient and low-loss optical phase modulation has been achieved and can be utilized for optical modulating and switching applications [1, 2]. Figure 1(a) shows a schematic of a III-V/Si hybrid MOS optical phase shifter. Driven by a positive gate voltage, electrons are accumulated on the III-V MOS interface, modulating the optical phase. The modulation efficiency $V_\pi L$ of a III-V/Si hybrid MOS capacitor is proportional to the oxide capacitance which is determined by the equivalent oxide thickness (EOT). By scaling the EOT to below 5 nm, a $V_\pi L$ smaller than 0.05 Vcm is expected. In our previous study, it was found that by introducing HfO_2 into the Al_2O_3 bonding interface, the void generation during wafer-bonding process was effectively suppressed. Moreover, the high k value of HfO_2 is beneficial for efficient EOT scaling. In this study, we presented a III-V/Si hybrid MOS capacitor with a thin capacitance equivalent thickness (CET) as small as 3.5 nm by employing HfO_2/Al_2O_3 stack for wafer bonding to enhance the modulation efficiency of the III-V/Si hybrid MOS optical phase shifter.

【Device structure】 Figure 1(b) shows a schematic of a wafer-bonded III-V/Si hybrid MOS capacitor. An Al_2O_3 layer was deposited on a III-V wafer, while a HfO_2/Al_2O_3 stack was deposited on a Si wafer. Then, the III-V and Si wafers were bonded together. After wafer-bonding, the InP substrate and etch-stop layers in the III-V wafer were removed by chemical etching. Finally, electrodes were evaporated on the III-V and Si wafers.

【Result and Discussion】 Figure 2(a) shows the capacitance-voltage (CV) characteristic of the wafer-bonded III-V/Si MOS capacitor. In this sample, 2.6-nm-thick HfO_2 and 2.4-nm-thick Al_2O_3 were used for wafer bonding. A small CET of 3.5 nm was successfully achieved. Figure 2(b) shows the simulated performance of a III-V/Si hybrid MOS optical phase shifter with a 3.5-nm-thick CET. A low $V_\pi L$ of 0.029 Vcm with a small absorption loss of 0.21 dB at π phase shift was predicted. As a result, we have successfully achieved the CET scaling for high-efficiency III-V/Si hybrid MOS optical phase shifter.

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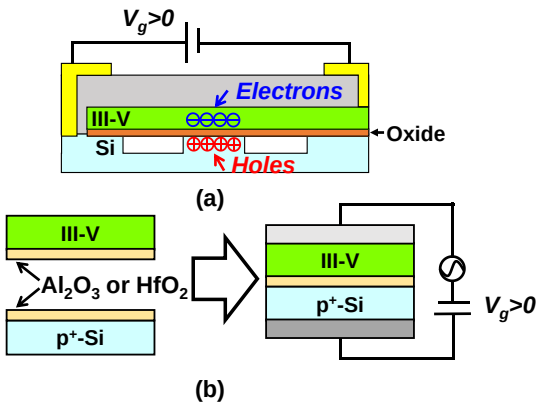

Fig. 1 (a) A schematic of the III-V/Si hybrid MOS optical phase shifter and (b) a schematic of III-V/Si hybrid MOS capacitor.

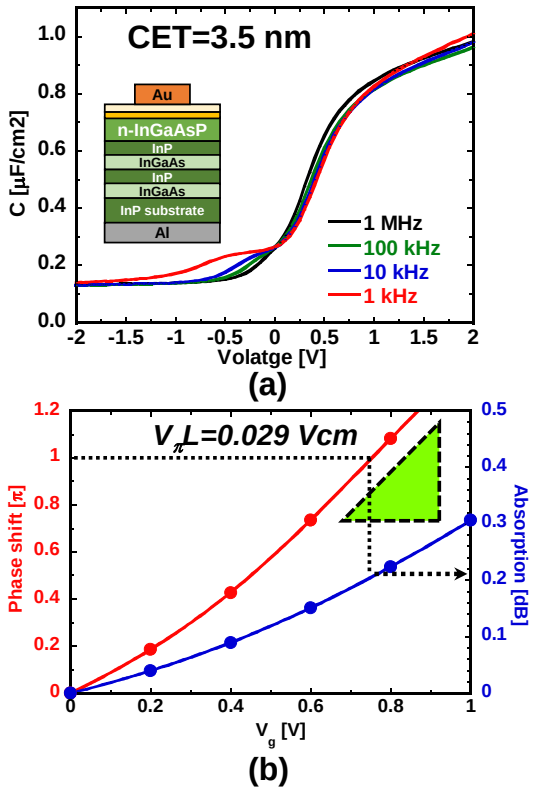

Fig. 2 (a) C-V characteristics of wafer-bonded III-V/Si hybrid MOS capacitor and (b) performance of III-V/Si hybrid MOS optical phase shifter with a 3.5-nm EOT.