Improvement of $Si_{0.78}Ge_{0.22}$ MOS interface properties by using TiN/Y_2O_3 gate stacks with TMA passivation

○ T.-E. Lee, K. Toprasertpong, M. Takenaka and S. Takagi
The University of Tokyo, Faculty of Engineering
E-mail: leete@mosfet.t.u-tokyo.ac.jp

1. Introduction

SiGe MOSFETs have stirred much attention as p-channel devices, because of the high hole mobility and the appropriate bandgap. However, the undesired formation of GeO_x in the interfacial layers (IL) can be regarded as an origin of the MOS interface degradation [1]. We have recently reported reduction in D_{it} by TiN/ALD Y_2O_3 gate stacks with PMA at 450°C [2, 3]. However, the further improvement of interface properties in the SiGe MOS gate stacks has not been fully obtained yet. In this study, we present a new passivation process by Trimethylaluminum (TMA) treatment prior to Y_2O_3 ALD in TiN/Y_2O_3/SiGe gate stack formation to achieve the SiGe MOS interfaces with lower D_{it}. The MOS interface properties and the physical origins of the interface improvements with optimized cycle number of TMA passivation are systematically examined.

2. Experiment

7-nm-thick non-doped $Si_{0.78}Ge_{0.22}$/p-type Si(100) wafers were cleaned by de-ionized water, acetone and diluted HF. Subsequently, 0, 10, 32 and 100 cycles of *in-situ* TMA passivation was performed before deposition of 7-nm-thick Y_2O_3 at 300°C by ALD using $(CpMe)_3Y$ and H_2O. Then, 40-nm-thick TiN gate electrodes were deposited by metal sputtering, followed by 100-nm-thick Al gate contact. Al was patterned by NMD-3. TiN were patterned by APM. PMA was performed for 1 min at 450°C in N_2 ambient. D_{it} was extracted by the conductance method with considerations of surface potential fluctuation.

3. Results and Discussion

The C-V curves of TiN/Y_2O_3 gate stacks with 0, 10, 32, and 100 cycles of TMA pre-treatments at 450°C of PMA are shown in Fig.1. It is found that D_{it}, hysteresis and the frequency dispersion are minimized at the 10 cycle TMA pre-treatment. The minimum value of D_{it} and CET at 100 kHz as a function of the TMA cycle number are shown in Fig. 2(a). The minimum value of D_{it} and C_{ox} have the similar TMA cycle dependence.

In order to understand the physical origin of the D_{it} reduction, XPS analyses were performed for the TiN/2-nm-thick Y_2O_3 stacks with the 0, 10, 32 and cycle TMA pre-treatments after PMA at 450°C and gate metal etching. The amounts of GeO_x and Al near the interfaces, shown in Fig. 2(b), were estimated from integrating the Ge^{3+} peak in Ge 3d and the Al^{3+} peak in Al 2p spectra. The amount of GeO_x in IL is reduced by TMA passivation, whereas the amount of Al^{3+} in IL increases with increasing the TMA cycle numbers. It is found that the optimum TMA condition minimizes the amount of GeO_x, leading to reduction in D_{it}. Further increase in the TMA cycle number leads to the increase in D_{it}. Since we have observed that D_{it} is higher in TiN/Al_2O_3 stacks than in TiN/Y_2O_3 stacks [2], this fact can be explained by the generation of D_{it} with too many Al atoms at the interfaces.

The TMA cycle number dependence of D_{it} and C_{ox} can be explained by the schematic diagram in Fig.3. This model suggests that 10 cycle TMA passivation reduces the amount of GeO_x with less amounts of Al^{3+}, whereas longer TMA treatments remain higher amounts of Al^{3+} in IL, leading to degradation of the MOS interface properties.

4. Conclusions

We have demonstrated the improvement of the TiN/Y_2O_3/$Si_{0.78}Ge_{0.22}$ MOS interfacial properties by using the optimum TMA pre-cleaning process and PMA at 450°C. It has been found the optimum TMA passivation can suppress the formation of GeO_x at the interfaces, leading to reduction in D_{it}.

Acknowledgements

This work was supported by JST CREST Grant Number JPMJCR1332, Japan and a Grant-in-Aid for Scientific Research (17H06148) from MEXT.

References [1] C.-H. Lee, et al., *VLSI Symp.*, 2016, pp. 36. [2] T.-E. Lee, et al., *VLSI Symp.*, 2019 [3] T.-E. Lee, et al., *Microelectronic Engineering* **214** (2019) 87.

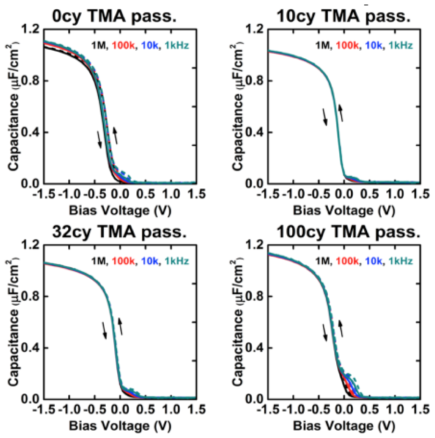

Fig.1: C-V curves of TiN/Y_2O_3/SiGe gate stacks with 0, 10, 32, 100 cycles of TMA passivation at 450°C of PMA.

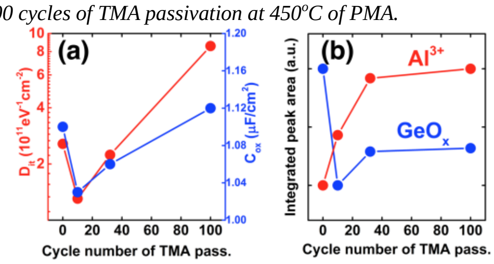

Fig.2: (a)D_{it} and CET (b)integrated peak area of GeO_x and Al^{3+} as a function of cycle number of TMA passivation.

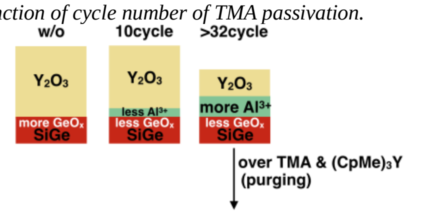

Fig.3: Schematic diagram of IL reaction a function of cycle number of TMA passivation followed by deposition of 7-nm-thick Y_2O_3.