Evaluation of Border Traps in Al₂O₃/GeO_x/p-Ge Stacks Using Deep-Level Transient Spectroscopy

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Introduction Ge is one of the candidate materials for the future metal-oxide-semiconductor field-effect transistors (MOSFETs) due to its high carrier mobility. For high mobility Ge MOSFET, stacked gate dielectric with thin Ge oxide interlayer, such as SiO₂/GeO₂ and Al₂O₃/GeO_x, has been studied actively [1,2]. On the other hand, in the case of Ge MOS, not only interface traps (ITs) but border traps (BTs) located in gate dielectric are also problematic because they degrades MOS characteristics and mobility. For deep understanding and performance improvement of Ge MOS device, both density and position of BTs in stacked gate dielectric should be clarified. However, in-depth study about BT in Ge stacked gate dielectric is limited [3]. Recently, we succeeded in separating the BT signal and IT signal using DLTS in SiO₂/GeO₂/Ge gate stacks grown by thermal and plasma oxidation [4]. In this study, we evaluated the density of IT (D_{it}) and density of BT (Nbt) in Al2O3/GeOx/p-Ge gate stacks grown by post plasma oxidation (PPO).

Experimental P-type (100) Ge substrate with doping concentration of 2.3×10¹⁶ cm⁻³ was used. After substrate cleaning, the first layer of Al₂O₃ was deposited at 300 °C by atomic layer deposition (ALD) for 3, 9, 14 and 20 cycles, followed by PPO by electron cyclotron resonance (ECR). Then, the second layer of Al₂O₃ was deposited at 300 °C by ALD for 25 cycles to suppress the current leakage. After 400 °C post-deposition annealing (PDA), TiN gate electrode was formed, followed by 350 °C post-metallization annealing (PMA). After Al deposition, electrodes are patterned. Next, 300 °C contact annealing (CA) was carried out, and the back contact was performed. The sample structure and GeO_x thickness information are shown in Fig. 1 and table 1, respectively. Both D_{it} and $N_{\rm bt}$ were characterized using DLTS [4].

Results and discussion Figure 2 shows the energy distribution of $D_{\rm it}$. In the region close to mid-gap, the thicker GeO_x contributes to the lower D_{it} . This is reasonable and commonly accepted [1], and the tendency also well agrees with the C-V characteristics (not shown). However, in the region close to valence band, the thicker GeO_x shows higher D_{it} . The reason is unclear yet. One possibility is that the mechanism is similar to the effect of defect termination by Al atom after post-metallization annealing (Al-PMA), so the ITs close to the valence band are passivated [5]. Figure 3 shows the temperature dependence of $N_{\rm bt}$. Here, we measured BT which affect capture/emission of hole in valence band of Ge. With decreasing thickness of GeO_x , N_{bt} firstly increases and then decreases. The measured depth of BT is approximately 0.4 nm when the tunneling barrier height is the band offset of GeO₂ and Ge [4]. The locations of detected N_{bt} are different. In the case of the thickest GeO_x (3 cycle-1st-Al₂O₃), BT in GeO_x is measured and the N_{bt} is comparable with our previous work about 1.8 nm-thick PPO GeO₂ [4]. In the case of 9 cycle-1st-Al₂O₃ corresponding 0.42 nm-thick GeO_x, BT located at the interface of Al_2O_3 and GeO_x is observed, and the N_{bt} is the highest in this study. If the 1st-Al₂O₃ is thicker (14-20 cycle) corresponding thinner GeO_x, the measured BTs are located in the Al_2O_3 layer and the N_{bt} is smaller than those of in GeO_x and Al₂O₃/GeO_x interface. Therefore, BT at Al₂O₃/GeO_x interface is the most serious for hole capture/emission in this stacked gate dielectric.

References [1] K. Hirayama *et al.*, Solid State Electron., **60**, 122 (2011). [2] R. Zhang *et al.*, IEEE Trans. Electron Devices, **59**, 335 (2012). [3] M. Ke *et al.*, APL, **109**, 032101 (2016). [4] W.-C. Wen *et al.*, JAP , **124**, 205303 (2018). [5] Y. Nagatomi *et al.*, Mater. Sci. Semicond. Process., **70**, 246 (2017).

