Performance enhancement of extremely thin body SiGe or Ge on insulator pMOSFETs fabricated by Ge condensation

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Background Ultrathin GOI and SGOI MOSFETs have attracted much attention as p-channel devices, because of the high hole mobility (μ_h) with suppression of short channel effects. Here, strain engineering also plays a key factor to enhance the performance of pMOSFET. On the other hand, compressive strain (ε_c) can be easily relaxed in high Ge fractions because of various crystal defects induced during the Ge condensation [1]. We have succeeded in suppression of strain relaxation thorough an improved condensation method, composed of slow-cooling and a thinned initial SiGe layer in the previous report [2]. By employing this method, μ_h of 467 cm²/Vs was obtained for 10 nm-thick GOI pMOSFETs with ε_c of ~1.75 % [2]. In this work, thinning of GOI and SGOI films fabricated by this condensation process is conducted down to 2 nm and compressively-strained 2nm-thick ETB GOI and SGOI pMOSFETs are shown to operate with higher μ_h than the reported ones. Also, the impact of the ETB thickness on the electrical characteristics is quantitatively studied.

[Experiments] In order to realize GOI pMOSFETs much thinner than in the our previous work [2], 100 % GOI and SGOI with Ge fractions of 70 % were thinned with atomic-scale thickness controllability by using ECR plasma oxidation/etching and TMAH wet etching, respectively. Fig. 1 (a) shows the GOI thickness (t_{GOI}), measured by ellipsometry, as a function of the number of ECR plasma oxidation/wet etching cycles. Fig. 1 (b) shows SGOI thickness (t_{SGOI}) as a function of etching time. The TEM images (Fig. 2) clearly show that 2.0-nm-thick GOI and 2.1-nm-thick SGOI (Ge 70 %) are uniformly fabricated without any visible defects. Fig. 3 shows measured ε_{e} as a function of t_{GOI} and t_{SGOI} . It is found that there is no strain relaxation down to 3 nm, while strain starts to get relaxed around 2 nm and is fully relaxed at 1 nm.

[Results] Fig. 4 shows the I_d - V_g characteristics of GOI pMOSFETs with changing t_{GOI} from 10 nm to 2 nm. We have demonstrated the operation of GOI pMOSFET with high on/off ratio and high mobility in this GOI thickness range. However, it is found that the peak hole mobility dramatically degraded at 2 nm because of thickness fluctuation scattering with ETB GOI films [3], as shown in Fig. 4. This result is also consistent with strain relaxation Fig. 3. Fig. 5 shows the μ_h -Ns characteristics of the (S)GOI MOSFETs with the Ge fractions of 100 % and 70 % as a parameter of t_{SGOI} down to 2 nm. The mobility degradation with reducing the channel thickness is mitigated by application of compressive strain. It is also confirmed that higher μ_h in higher Ge fractions is maintained down to t_{SGOI} of 2 nm.

We have demonstrated ETB (S)GOI MOSFETs with the body thickness from 10 to 2 nm. The Conclusion high μ_h due to high ε_c has been obtained by the combination of the improved Ge condensation method. **[References]** [1] S. Nakaharai et al., APL **83**, 3561 (2003) [2] K.-W. Jo et al., APL **114**, 062101 (2019) [3] X.

Yu et al., IEDM 20 (2015)

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Fig. 1 t_{GOI} as function of cycles (a) t_{SGOI} as function of etching time (b)



Fig. 2 TEM of ETB GOI 2 nm (a), and 2.1 nm (b)

S 2.0 strain 1.3 Ge ε_{in} Compressive 100 % 1.7 % 85 % 1.8 % 70 % 1.9 % ⁴⁹ % ^{1.7} % 2 nm 0 ! 10 (S)GOI thickness (nm)

Fig. 3 t_{SGOI} dependence of ε_{c}

