Epitaxial Growth Technique using InP-on-Insulator towards III-V/Si Photonic Integrated Circuits

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1. Introduction

The explosive increase in internet traffic requires cost-effective optical networks between and within data-centers. However, to build these cost-effective networks, we need to fundamentally change how we manufacture InP-based photonic devices. InP/Si photonic integrated circuits (PICs) using silicon-photonics technologies are promising for such short-distance communications. Silicon-photonics technologies enable the integration of several functional devices except for lasers on a single compact chip, which can dramatically reduce assembly and packaging costs. Therefore, a cost-effective way to integrate InP-based active devices on a silicon-based platform is strongly desired. In this context, we have developed a new III-V/Si integration scheme in which an InP membrane is directly bonded to SiO_2/Si substrate (InP-on-insulator) as an epitaxial template. Compared with a direct-growth scheme, this scheme solves the problems of lattice mismatch and the formation of anti-phase boundaries. In addition, we overcame the crystal degradation due to the difference in coefficient of thermal expansion, by keeping the III-V layer thickness at less than ~400 nm. Using this technique, we have so far developed energy-efficient >25-Gbit/s directly modulated lasers (DMLs) [1, 2]. Here, we present the fabrication of a DML array for wavelength-division multiplexing (WDM) application. InGaAlAs MQWs were grown on an InP-on-insulator using a selective growth mask to obtain different gain spectra [3]. We have fabricated a wide-wavelength range DML array that can be operated with 25.8-Gbit/s NRZ signal.

2. Device fabrication

Figure 1(a) depicts the fabrication procedure. First, a 2-inch InP epitaxial wafer that includes an InP membrane layer and InGaAs cap layer is directly bonded to a thermally oxidized silicon wafer using oxygen-plasma assisted bonding. Next, an InP-on-insulator is obtained by removing the InP wafer after the bonding. After that, selective-growth SiO_2 masks with different mask width, *w*, are formed on the InP membrane. The selective epitaxial growth of six-period InGaAlAs/InGaAlAs MQWs is carried out using MOVPE. The photoluminescence (PL) spectra in Fig. 1(b) show that the crystal quality of the selectively grown MQWs is as high as that of those grown on a standard InP substrate. We then fabricated an eight-channel membrane DML array. Figure 1(c) depicts a bird's eye view of a discrete DML. We used various techniques that we have previously developed, including epitaxial regrowth for buried heterostructures (BHs), ion-implantation and thermal diffusion for lateral p-i-n junctions, dry-etched surface grating for single-mode operation, and SiO_x spot-size converter for efficient fiber coupling [1, 2, 4]. Figure 2 characterizes eight-channel membrane DMLs. We successfully controlled the detuning between the PL and lasing wavelength. Thanks to the suitable gain wavelength for each channel, we observed clear eye-opening at 25.8-Gbit/s NRZ operation for both shorter- and longer edge channels.

3. Conclusions

We have developed a selective epitaxial growth technique using InP-on-insulator, which enables wide-wavelength-range DML arrays on silicon. The results point to the possibility of using this technique to fabricate InP/Si PICs for datacenter applications.

References

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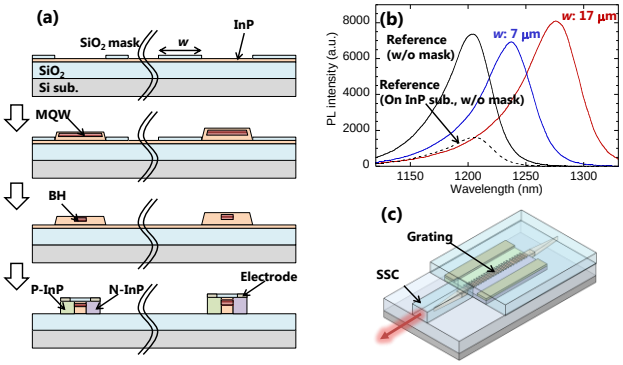

Fig. 1 Overview of selectively-grown membrane DML.

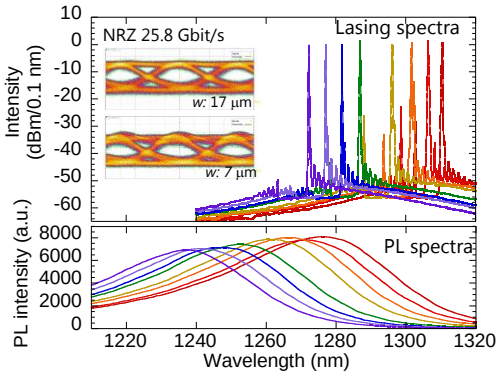

Fig. 2 Lasing characteristics of membrane DML array.