SiO_2/4H-SiC バンドアライメントに結晶面の違いと酸化後アニールプロセスの違いが与える効果

Significant effects on SiO_2/4H-SiC band alignment induced by the difference of employed crystal face and post-oxidation annealing processes

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[Introduction] To improve the quality of SiO_2/4H-SiC interface, several kinds of post-oxidation annealing (POA) process are used. For Si-face 4H-SiC, it is already well known that NO-POA is an effective method to reduce D_{it}. However, after NO-POA, there is a negative shift of threshold voltage. Therefore, as one possible origin of that phenomenon, we reported about the band alignment shift induced by NO-POA [1]. Furthermore, it would be also important to see the crystal face dependence of such influences of POA on the band alignment. In this work, we compared the effect of POA on the band alignment shift of Si-face and C-face. Especially we focused on the effect of Wet-POA as an annealing method of C-face samples because Wet-POA is already confirmed as an effective method for C-face MOS capacitors [2].

[Experiments] N-type 4H-SiC Si-face and C-face wafers with epitaxial layers (N_D~1.0×10^{16} cm^{-3}) were used as the substrates. After HF cleaning, samples were dry oxidized at 1300°C with 100% and 2% oxygen (diluted with N_2) to grow a SiO_2 layer for Si-face and C-face substrates, respectively. The thickness of the layer was controlled by the oxidation duration. After dry oxidation, NO-POA (1150°C, 33% NO with N_2, 0.5~8 h) processes were performed for both substrates and wet-POA (p_{H_2O}: 0.2 atm with N_2 as a carrier gas, 800~1000°C) processes were performed for C-face samples. After deposition of the electrodes (top: Au, bottom: Al), we measured C-V characteristic at 1 MHz and V_{FB} was extracted for each sample.

[Results & Discussions] Fig. 1 shows the T_{ox} (CET) dependence of V_{FB} of samples with different POA conditions. The inset shows the C-V curve of C-face MOS capacitor with Wet-POA. The improved interface quality was observed after Wet-POA, especially for the case of 900°C. Also, we confirmed the improved interface quality after NO-POA on both crystal faces. V_{FB} was reasonably extracted since all the samples show nearly ideal curves with small frequency dispersions. From **Fig. 1**, a larger slope was observed on C-face than on Si-face, which means more fixed oxide charges at the interface. The offset observed by the extrapolation of the slope to CET=0, which gives the value after the removal of the shift due to the fixed charges, show significant influences of both the employed annealing processes and crystal faces. As we already reported [1], such difference of the offsets is explainable by assuming the formation of a dipole layer at the interface with various strength. So, we estimated the conduction band offset of the MOS interface (ΔE_c) by measuring the valence band offset from XPS valence band spectra. For some samples, the extracted ΔE_c was confirmed to be consistent with the value determined from F-N tunneling currents. Note that we've confirmed from O1s loss spectrum that SiO_2 bandgap is not affected by either POAs or crystal faces. **Fig.2** shows the change of ΔE_c after Wet-POA on C-face. Interestingly, there was a large decrease in ΔE_c after Wet-POA, even though the origin of this dramatic decrease is not clarified so far. Finally, we compared ΔE_c after NO-POA on Si-face and C-face, together with the one after Wet-POA on C-face (**Fig.3**) When we compare the ΔE_c of the dry oxidized samples, the intrinsic difference of ΔE_c between Si-face and C-face was observed, which is approximately consistent with a previous report [3]. After NO-POA, ΔE_c increased on Si-face but decreased on C-face. Moreover, after Wet-POA on C-face, there was furthermore reduction of ΔE_c. Therefore, we can conclude that the observed large difference of ΔE_c between Si-face and C-face after POA would be originated from both (i) the intrinsic difference of crystal face and (ii) the difference of the POA effects, especially due to the significant effects of Wet-POA uniquely on C-face.

[Conclusions] There was an intrinsic difference of conduction band offset between the Si-face and C-face 4H-SiC MOS interfaces. Moreover, the effect of POA on the band alignment shift also varied according to the crystal face. On Si-face, there was a rise of ΔE_c after NO-POA and increased more with increasing NO-POA duration, whereas the Wet-POA on C-face induced a significant decrease of ΔE_c.

Acknowledgments. This work was partly supported by CSTI, Cross-ministerial Strategic Innovation Promotion Program, "Next-generation power electronics" (funding agency: NEDO), and by JSPS KAKENHI. **Reference.** [1] T.H. Kil et al., JSAP Spring Meeting (2019) [2] K. Kita et al., Microelectron. Eng. (2017) [3] H. Watanabe et al., Mater. Sci. Forum (2011)

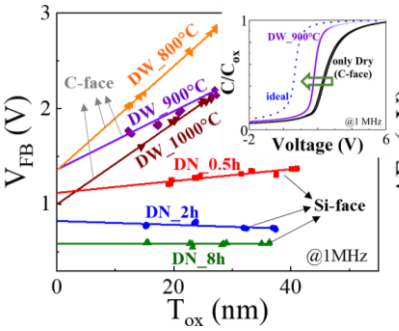

Fig.1 V_{FB}-T_{ox} graph of MOS capacitors after POA (inset: C-V curve of DW sample)

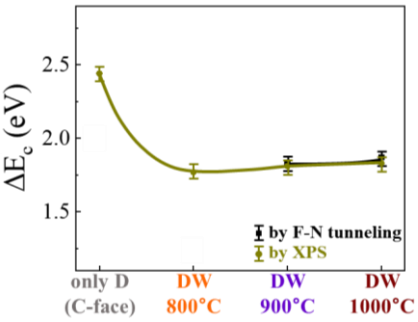

Fig.2 Estimated ΔE_c of Wet-POA samples (C-face) by F-N tunneling and XPS

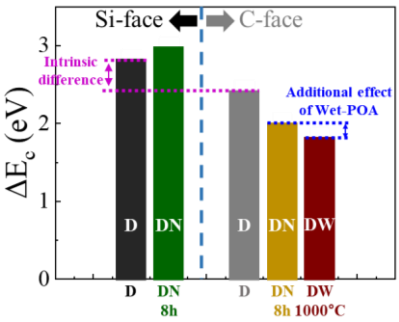

Fig.3 Estimated ΔE_c by XPS after various kinds of POA on Si-face and C-face samples