Vertical Enhancement-Mode $\beta$-Ga$_2$O$_3$ MOSFETs with a Current Aperture
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Normally-off vertical power switches enable superior field termination and current drive at the device level while ensuring fail-safe operation and simplified designs at the system level. We have demonstrated depletion-mode (D-mode) vertical $\beta$-Ga$_2$O$_3$ (Ga$_2$O$_3$) MOSFETs that capitalize on ion-implantation technologies for Si donor and N acceptor doping of Ga$_2$O$_3$ [1]. Based on this highly manufacturable structure, this paper presents enhancement-mode (E-mode) vertical Ga$_2$O$_3$ MOSFETs by engineering the channel doping to obtain a positive threshold voltage ($V_T$) without requiring fundamental process modifications.

The E-mode vertical Ga$_2$O$_3$ MOSFET consisted of a 9-µm-thick Si-doped $n$-Ga$_2$O$_3$ drift layer with a donor density ($N_D$) of $1.5\times10^{16}$ cm$^{-3}$ grown by halide vapor phase epitaxy (HVPE) on an $n$'-Ga$_2$O$_3$ (001) substrate (Fig. 1) [2,3]. A buried current blocking layer (CBL) for source–drain isolation was formed by N-ion (N ++) implantation doping. To recover implantation damage and activate N as a deep acceptor, thermal annealing was performed at 1100°C for 30 min in N$_2$. Subsequent Si-ion (Si +) implantations formed the electron channel ($N_D=5\times10^{17}$ cm$^{-3}$, 0.15-µm-thick box profile) and source contact layers that were activated at 950°C and 800°C, respectively, for 30 min in N$_2$. In equilibrium, the channel was fully depleted by both the $n$-channel/CBL junction potential and the surface potential, giving rise to normally-off FET operation whereby electrons were induced in the channel layer by applying a positive gate voltage ($V_G$). A 50-nm-thick Al$_2$O$_3$ gate dielectric was then formed by plasma-assisted atomic layer deposition. Ti/Au and Ti/Pt/Au were used for the ohmic and gate electrodes, respectively. Finally, Ti/Au source probing pads were deposited on Al$_2$O$_3$ for low pad leakage. The MOSFET had an aperture size of 20 µm and a channel length of 5 µm.

At $V_G=+6$ V, the E-mode MOSFET delivered an $I_D$ of 0.027 kA/cm$^2$ (normalized to the Si channel implant area) [Fig. 2(a)], which was almost equal to 1/10 of those of D-mode MOSFETs with a channel $N_D$ of $1\times10^{18}$ cm$^{-3}$ fabricated concurrently on the same wafer. While the D-mode devices exhibited linear $I_D$ turn-on with drain voltage ($V_D$) as expected for normal transistor operation, the E-mode device displayed diode-like non-linear behavior that indicated the presence of an electron barrier in the current path. At $V_D=20$ V, the E-mode MOSFET showed a $V_T$ of +3.2 V (obtained by linear extrapolation of the transfer curve toward the $V_G$ axis), a large drain current ($I_D$) on/off ratio exceeding $7\times10^6$, and a small $I_D$-$V_G$ hysteresis of <0.4 V [Fig. 2(b)]. The off-state breakdown voltage of the E-mode MOSFET measured at $V_G=0$ V was 260 V.

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Fig. 1. Cross-sectional schematic of E-mode vertical MOSFET. The aperture and source widths were 200 µm.

Fig. 2. (a) $I_D$-$V_D$ ($\Delta V_G = +1$ V) and (b) $I_D$-$V_G$ ($V_D = 20$ V) characteristics of E-mode MOSFET.