Formation of fine-textured surface on as-cut crystalline silicon wafers by microparticle-assisted texturing (MPAT) process

Cong Thanh Nguyen, Keisuke Ohdaira, and Hideki Matsumura
Japan Advanced Institute of Science and Technology (JAIST)
E-mail: nguyen.cong.thanh@jaist.ac.jp

Recently heterojunction back-contact (HBC) crystalline silicon (c-Si) solar cells with efficiency >26% have been developed [1]. Reducing the thickness of c-Si to <100 µm is one of the keys to low-cost solar cells. Usually, the surface of the c-Si is textured for good light confinement and improvement of the cell efficiency. On such thin c-Si wafers, reducing the size of textures is necessary to minimize c-Si losses by texturing process and to keep robust property during cell fabrication. To obtain the textures with a size <2 µm using alkaline anisotropic etching, we have already established "microparticle-assisted texturing" (MPAT) process. However, up to now, the MPAT process has been being applied to only mirror-polished c-Si wafers [2]. Usually in solar cell manufactures, as-cut wafers are directly dipped into texturing solutions for reducing the cost. Therefore, in this work, we aimed to investigate the feasibility of the MPAT process on the as-cut c-Si wafers. Fundamentals and advantages of the MPAT process will be revealed.

We employed as-cut c-Si wafers used for solar cells. Owing to a cutting process, a saw-damaged layer with a depth <6 µm exists on both sides of the wafers, as shown in Fig. 1.

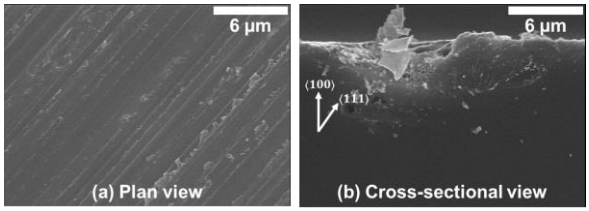

Fig. 1: Scanning electron microscopy (SEM) images of the as-cut c-Si wafers.

In order to reduce the cost, the saw-damaged layer and the texturing process should be done in only one step, in which the wafers were simply dipped into an alkaline texturing solution mixed with glass microparticles, so-called the MPAT solution [2]. Figure 2 shows the flow of the texturing process. Detailed conditions of the MPAT process were also reported in Ref. [2].

Using the MPAT process, in the present case, we can make the texture with a size down to less than several µm, as shown in Fig. 3. Minimal optical reflectivity of the textures ~7% can be obtained. After the formation of the textures, we also developed a suitable cleaning procedure to obtain high-quality surface passivation by using well-known catalytic chemical vapor deposition (Cat-CVD) silicon nitride (SiN_x)/ amorphous silicon (a-Si) stacked layers. Effective minority carrier lifetime (τ_{eff}) is ~6 ms. The value is equivalent to that obtained for textures made from mirror-polished c-Si, The detailed Cat-CVD conditions for the SiN_x/a-Si stacks were well established [2-4].

Fig. 2: Flow of the MPAT process followed by cleaning and surface passivation

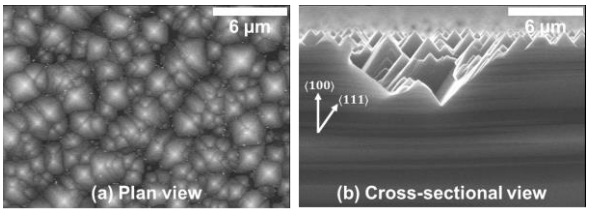

Fig. 3: SEM images of the textured c-Si surface formed by the MPAT process.

In summary, we can control the texture size by using the MPAT process on the as-cut c-Si wafers Cleaning and high-quality surface passivation were also possible. Therefore the MPAT process is feasible for industrial solar cell fabrication.

Acknowledgments

This work is supported by New Energy and Industrial Technology Development Organization (NEDO), Japan

References

[1] K. Yoshikawa, H. Kawasaki, W. Yoshida, T. Irie, K. Konishi, K. Nakano, T. Uto, D. Adachi, M. Kanematsu, H. Uzu, and K. Yamamoto, Nat. Energy **2**, 17032 (2017).

[2] C.T. Nguyen, K. Koyama, H.T.C. Tu, K. Ohdaira, and H. Matsumura, in *J. Mater. Res.* (Cambridge University Press, Hawaii, 2018), pp. 1515–1522.

[3] K. Koyama, K. Ohdaira, and H. Matsumura, Appl. Phys. Lett. **97**, 082108 (2010).

[4] C.T. Nguyen, K. Koyama, K. Higashimine, S. Terashima, C. Okamoto, S. Sugiyama, K. Ohdaira, and H. Matsumura, Jpn. J. Appl. Phys. **56**, 056502 (2017).