Scalability Study on Ferroelectric-HfO_2 Tunnel Junction Memory

IIS, Univ. of Tokyo (D2)Fei Mo, (M2)Yusaku Tagawa, Takuya Saraya, Toshiro Hiramoto and Masaharu Kobayashi

E-mail: mofei@nano.iis.u-tokyo.ac.jp

Internet of things (IoT) devices need extreme low power Non-volatile memories (NVMs) to store, communicate and process data at low cost because of their energy harvesting. Ferroelectric tunnel junction (FTJ) memory has become one of the promising candidates for IOT application because of its non-destructive readout, low voltage operation and high on/off current ratio [1].

In this paper, we have proposed a numerical simulator for HfO_2-based FTJ memory based on Non-Equilibrium Green Function (NEGF) method [2] and self-consistent potential, investigated scalability and design a guideline of HfO_2-based Metal-Ferroelectric-Insulator-semiconductor (MFIS) structure FTJ. We fabricated an MFIS FTJ and calibrate the simulator by experimental data. We have defined the device structure and parameters of simulated MFIS FTJ. External bias voltage (V_a), grid length for calculation(a) and thickness of each layer are defined. Our proposed simulation framework consists of two parts: (1) self-consistent potential calculation sub-module and (2) current density calculation main-module. For potential calculation, we consider external applied voltage, voltage across each layer, band offset, and build-in potential. For current calculation, we use NEGF method at each bias voltage to calculate the tunnel current.

Simulation results and discussion

We fabricated MFIS structure FTJ with Al replacement process and measure the I-V curve to calibrate our simulation framework [3]. Experimental data and simulation results have a good fit at both ON and OFF state by using default simulation parameters which were obtained from TEM measurement and Positive-Up-Negative-Down (PUND) measurement. We compared the MFIS and MFIM structure FTJ. The ON current of MFIM and MFIS structure FTJs are nearly the same, while, MFIS FTJ has higher TER ratio than MFIM structure due to the large asymmetry of dielectric screening property in electrodes. Before investigating the scalability potential of MFIS FTJ, we examine the influence of P_r, N_d, FE layer(t_{FE}) and interfacial layer(t_{ox}). As P_r decreases, ON current remains nearly constant, while OFF current is more influenced and increases. TER ratio is reduced. As N_d decreases, ON current remains nearly constant, while OFF current is more influenced and decreases. TER ratio is improved. Then, we examined FE and interfacial layer thickness dependence of ON current and TER ratio. Here we introduce empirical relationship between P_r and t_{FE}: P_r is proportional to t_{FE}. As t_{FE} and t_{ox} are thinned down, ON current increases. However, because of the smaller P_r, TER ratio becomes small. Based on the simulation results, we can obtain High read current, high TER and low depolarizing field by adjusting bottom semiconductor electrode property and reducing the thickness of ferroelectric layer. Fig. 1 and Fig. 2 show TER ratio and required t_{FE} for 10 nA and 100 nA target I_{read} as a function of FTJ cell size. I_{read}=10nA and TER ratio >1can be obtained down to 20nm size with default N_d=3e19cm^{-3}. I_{read}=100nA and TER ratio >1 is challenging because of the extreme thin film but can be obtained down to 20nm with technologically possible FE thickness ~1.5nm by decreasing N_d to compensate TER ratio.

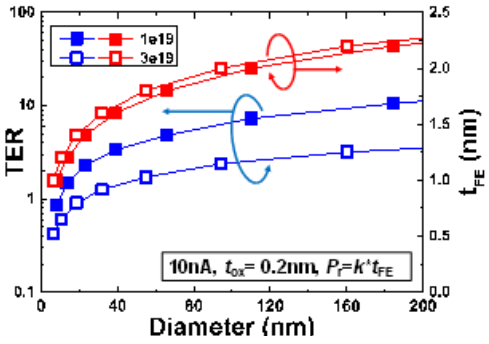

Fig.1 TER ratio and required t_{FE} versus FTJ size to target I_{read} = 10nA at ON state

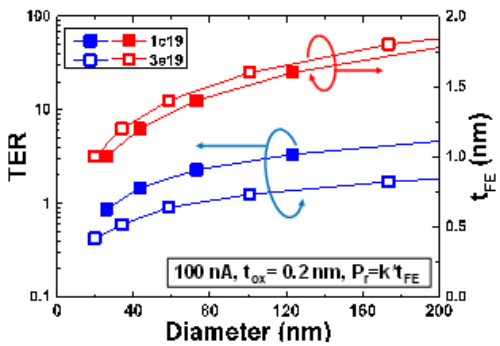

Fig.2 TER ratio and required t_{FE} versus FTJ size to target I_{read} = 100nA at ON state.

Reference: [1]Vincent Garcia et al, Nature Communication, (2014). [2] Supriyo Datta, "Quantum Transport: Atom to Transistor"(2006) [3]Masaharu Kobayashi et al, IEEE SNW 2018