NO アニールされた SiO_2/4H-SiC MOS キャパシタの フラットバンド電圧の負方向への異常なシフト

An anomalous negative shift of flat-band voltage of NO annealed SiO_2/4H-SiC MOS capacitors

Dept. of Materials Engineering, The Univ. of Tokyo, ◦Tae-Hyeon Kil, Atsushi Tamura and Koji Kita
E-mail: thkil@scio.t.u-tokyo.ac.jp

[Introduction] NO post-oxidation annealing (NO-POA) process is a beneficial method to reduce the D_{it} of SiO_2/4H-SiC interface and improve the MOSFET performance [1]. One of the drawbacks of this POA is the negative shift of threshold voltage. However, the origin of this phenomenon is not clarified yet. In this work, we investigated the effect of NO-POA with varying durations on flat-band voltage (V_{FB}) of MOS capacitors. With systematic analysis of V_{FB}-CET relationship, the fixed oxide charge at the interface, dipole effect or other unknown effects can be distinguished.

[Experiments] N-type 4H-SiC Si face wafers with epitaxial layers (N_D=1.1×10^{16} cm^{-3}) were used as the substrates. After HF cleaning, samples were dry oxidized at 1300℃ to grow a SiO_2 layer. The thickness of the layer was controlled by the oxidation duration. After dry oxidation, NO-POA processes at 1150℃ in the ambient of NO:N_2=1:2 were performed for different durations (from 30 min to 8 hours). Finally, electrodes were deposited, Au for the gate and Al for the bottom. From the C-V characteristic measured at 1 MHz or 1 kHz, V_{FB} was determined for each sample.

[Results & Discussions] Fig.1 shows the C-V curves of SiO_2/4H-SiC capacitors with NO-POA for various durations. V_{FB} for all the samples were reasonably extracted since they show nearly-ideal curves with small frequency dispersions. **Fig.2** shows the CET dependence of V_{FB} of samples with different NO-POA duration. From the V_{FB}-CET graph, fixed oxide charges at the interface (Q_0) can be known by the slope of the line. With increasing NO-POA duration (from 30 min to 8 hours), the slope of the line decreased, which means the reduction of the Q_0 from -1×10^{11} cm^{-2} to less than 10^{10} cm^{-2}. Also, the dispersion of V_{FB}, which means the gap between V_{FB} measured at 1 MHz and 1 kHz decreased with increasing NO-POA duration. From the extrapolation of each line to CET=0 gives the V_{FB} value without the effects of fixed charges. As can be seen clearly from the variation of the offsets for the lines with different POA durations (**Fig.3**), there must be an additional mechanism to cause the V_{FB} negative shift (more than 0.5 V) by 8 hours of NO-POA other than fixed charge elimination, which means the change of the dipole effect or other unknown effect by the NO-POA. This anomalous negative shift would be related to the nitrogen concentration of SiC side or SiO_2 side of the interface. From the gate leakage current measurement, it is confirmed that Fowler-Nordheim tunneling barrier height (~2.7 eV) does not significantly affected by NO-POA duration. Ideal V_{FB} can be estimated reasonably in the range of 0.7 V to 1 V considering the work function of Au.

[Conclusions] With increasing NO-POA duration after dry oxidation, fixed oxide charges at the interface decreased to less than 10^{10} cm^{-2}. Moreover, there was an anomalous negative shift of extrapolated V_{FB} (more than 0.5 V), which would be related to the nitrogen concentration at the interface.

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Reference. [1] K. McDonald et al., Journal of Applied Physics 93, 5 (2003)

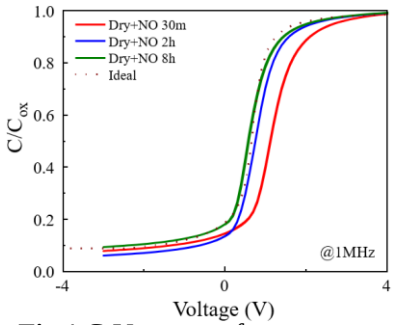

Fig.1 C-V curves of SiO_2/4H-SiC MOS capacitors

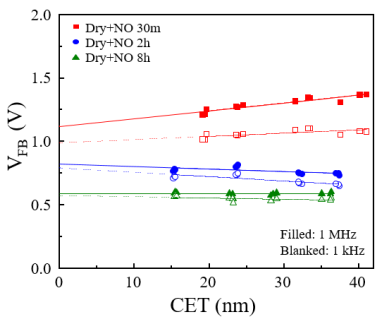

Fig.2 V_{FB}-CET graph of NO-POA samples with varying NO-POA duration

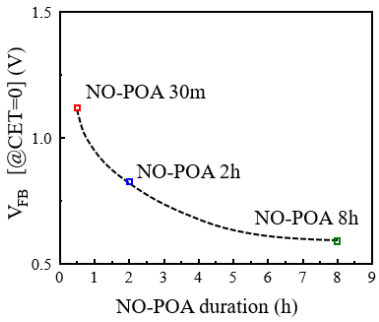

Fig.3 Extrapolated V_{FB} values with varying NO-POA durations