The Schottky barrier height modulation of Pd_2Si/p-Si(100) diodes by dopant segregation process

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1. Introduction

The source and drain (S/D) engineering of MISFETs is necessary to integrate the high-k gate insulators in the low thermal budget gate-first CMOS fabrication. The Schottky barrier (SB) S/D utilizing metal silicides could replace the conventional S/D to realize the low temperature process [1]. However, one of the challenges in this process is the use of different silicides in nMISFET and pMISFET that complicates the device fabrication [2]. As such, the dopant segregation (DS) process was introduced to modulate the SB height (SBH) to be able to use single silicide material for both devices. We have reported that Pd_2Si/n-Si(100) diodes with low SBH to hole of 0.20 eV was realized by DS process with boron (B) dopants (B-DS) [3]. In this work, the modulation of the SBH of Pd_2Si/p-Si(100) diodes with phosphorus (P) dopants (P-DS) was investigated for future applications in the nMISFET fabrication for the low thermal budget gate-first CMOS.

2. Experimental Procedure

The p-Si(100) substrates were cleaned using SPM and DHF. The SiO_2 field oxide was formed by wet oxidation at 1050 °C. The 100x100 μm^2 active regions were formed by photolithography and wet etching. The 30-nm-thick Pd was formed by RF magnetron sputtering with 4.4 sccm Ar gas, 120 W RF power at 0.67 Pa and room temperature (RT). The 10-nm-thick TiN encapsulating layer was in-situ deposited with 3.6/0.4 sccm Kr/N_2, 100 W RF power at 1.05 Pa and RT. The ion implantation (I/I) of phosphorus dopants at 25 keV with ion doses of 1-5x10^{15} cm^{-2} were performed for the DS process. It was followed by the single step annealing for the silicidation and the DS process under 1 SLM N_2 at 500 °C/1 min using RTA. The TiN layer was etched by NH_4OH:H_2O_2 (1:1) solution and the unreacted Pd was selectively etched using diluted aqua regia both at 50 °C. Finally, the Al back contact was deposited by evaporation. The sheet resistances were measured by 4-point probe. The J-V characteristics were obtained using Agilent 4156C and the SBHs were extracted using the thermal emission method.

3. Results and Discussion

Figure 1 shows the sheet resistances of the Pd_2Si without DS, with P-DS and with B-DS. The sample without DS process showed the lowest sheet resistance of 10.4 Ω/sq after the selective etching while the sample with P-DS process showed 11.4 Ω/sq for ion dose of 1x10^{15} cm^{-2}. Meanwhile, the Pd_2Si/n-Si(100) with B also showed sheet resistance of 11.4 Ω/sq. Although the sheet resistances of the samples with DS process are slightly higher compared to those without the DS process, the differences are small. In this case, the formation of Pd_2Si and its crystallinity were not degraded by the I/I process for both P and B. Figure 2 shows the J-V characteristics of the SB diodes. The diodes without DS process showed Ohmic characteristics with high forward and reverse currents. As the P ion concentration was increased, the reverse current decreases. In this case, the DS process with P dopants modulated the SBH to hole where the increase in the dopant concentration lowered the reverse current indicating that the SBH to hole was increased (SBH to electron was decreased). The extracted results show that the SBH to electron was decreased from 0.67 eV to 0.61 eV as the ion dose was increased.

4. Conclusions

The effects of the DS process on the electrical properties of Pd_2Si/p-Si(100) were investigated. As a conclusion, the SBH to electron was lowered to 0.61 eV by using the DS process. Increasing the amount of dopant decreases the SBH to electron of the Pd_2Si/p-Si(100) diodes.

5. Acknowledgments

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6. References

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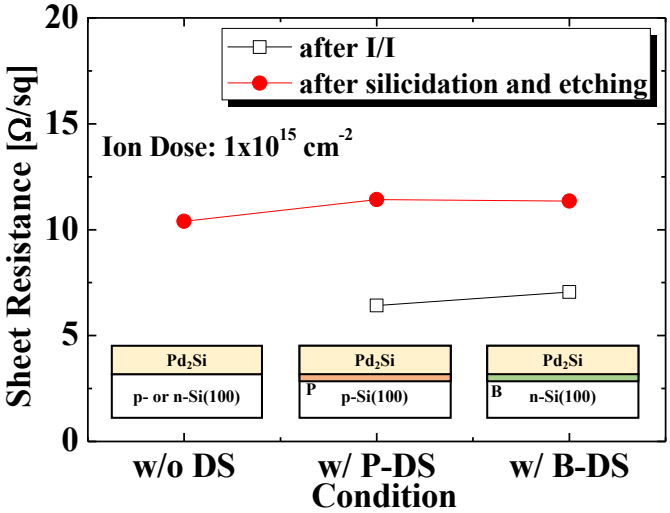

Fig. 1 Dependence of sheet resistance on process conditions.

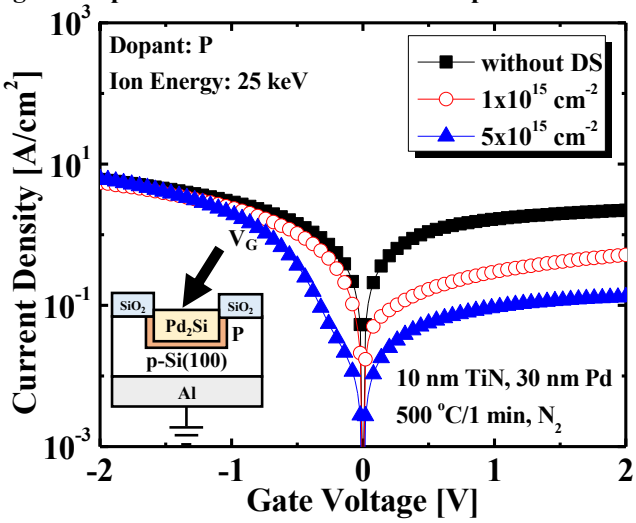

Fig. 2 The J-V characteristics of the SB diodes with P-DS.