Development of hydrogenated diamond triple-gate fin-type MOSFETs

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Thanks to its extraordinary intrinsic properties, wide bandgap semiconductor diamond is promising to fabricate electronic devices for low power-loss, high-power, high-frequency, and high-temperature applications. Recently, hydrogenated diamond (H-diamond) surface channel based metal-oxide-semiconductor field-effect transistors (MOSFETs) have been developed greatly. However, lack of large-area commercially available wafers hinders them for future practical applications. To resolve this issue, we have tried to downscale device size and to enhance electrical properties of the H-diamond MOSFETs to meet requirement of small area wafers. The triple-gate fin-type H-diamond MOSFET has been fabricated successfully [1]. Since holes in the fin channel can travel at both planar and lateral sides, current output and extrinsic transconductance of the fin-type MOSFET are much higher than those of the planar-type MOSFET at the same device area. However, some issues for the triple-gate fin-type H-diamond MOSFETs still exist. Fabrication process of them is quite complicated, leading to degradation of electrical properties and difficulty to repeat the experiment by other researchers. Additionally, ratio between height of lateral side and width of planar side for each fin is only 0.57, which means that the advantage of fin channel is not fully utilized. In this study, we have simplified the fabrication process for the triple-gate fin-type H-diamond MOSFETs and increased the ratio between height of lateral side and width of planar side for each fin to be 1.45 for further enhancing device current output at the same device area.

Figures 1(a) and 1(b) show surface morphologies of the planar-type and triple-gate fin-type H-diamond MOSFETs, respectively. Schematic diagrams for the planar-type and fin part of the triple-gate H-diamond MOSFETs are shown in Figs. 1(c) and 1(d), respectively. Gate width (W_G) for both planar-type and triple-gate MOSFETs is the same of 25.8 μm. Gate length (L_G), interspace for gate-to-source, and interspace for gate-to-drain are 4.2, 1.7, and 3.3 μm for the planar-type MOSFET, respectively. There are three fins for the triple-gate MOSFET. Each fin width and length are 2.0 and 20.2 μm, respectively. Interspace between two fins is 4.9 μm. Due to cover-area non-uniformity of photoresists during the formations of gate oxide and cover metals, the L_G, interspace for gate-to-source, and interspace for gate-to-drain are different for the triple-gate MOSFET in the planar and the fin parts. For the planar part, they are the same with those of the planar-type H-diamond MOSFET. For the fin part, they are 2.5, 2.4, and 3.7 μm, respectively. Fig. 1(e) demonstrates height (2.9 μm) of lateral side for the fin-channel by measuring the crossed key-pattern whose scanning electron microscopy (SEM) image is shown in the inset of Fig. 1(e). The ratio between height of lateral side and width of planar side for each fin can be calculated to be 1.45, which is much higher than the previous report of 0.57 [1]. Electrical properties of the planar-type and novel triple-gate fin-type H-diamond MOSFETs will demonstrated during the conference.

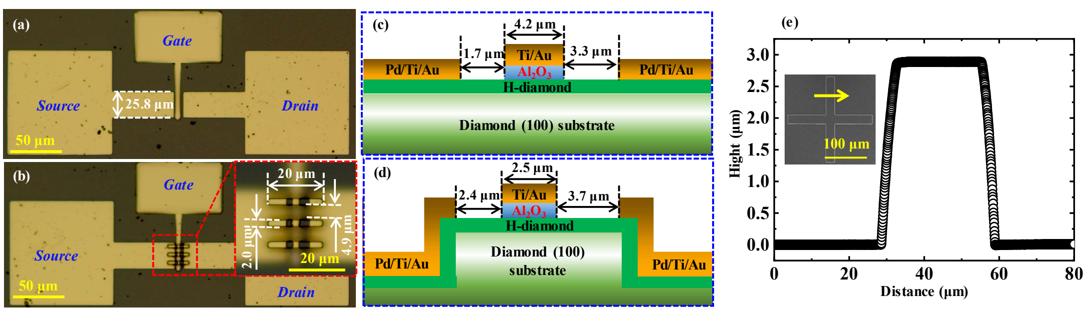

Fig.1 (a) and (b) Surface morphologies of planar-type and triple-gate fin-type H-diamond MOSFETs, respectively. Inset in Fig. 1(b) shows magnified fin part for the triple-gate MOSFET. (c) and (d) Schematic diagrams of planar-type and fin part of the triple-gate H-diamond MOSFETs, respectively. (e) Height of lateral side for the fin-channel confirmed by measuring the crossed key-pattern using a 3D-measurement laser microscopy system. Inset in Fig. 1(e) shows SEM image of the crossed key-pattern.

Reference

[1] J. W. Liu, H. Ohsato, X. Wang, M. Y. Liao, and Y. Koide, Sci. Rep. **6**, 34757 (2016).