Impact of metal gate electrodes on electrical properties of $Y_2O_3/Si_{0.78}Ge_{0.22}$ gate stacks

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1. Introduction

A SiGe MOSFET is a promising solution to realize high performance LSIs under the traditional scaling by the Moore's law. Strained SiGe grown on Si has larger hole mobility and smaller hole effective mass than Si. A strong concern on SiGe pFETs is the relatively high interface trap density (D_{it}) at SiGe MOS interfaces, which might be attributed to the undesired GeO_x formation in interfacial layers (IL)[1]. For high-k materials, Y_2O_3-based materials are promising for superior SiGe MOS interfaces [2]. We have found that increasing post metal annealing (PMA) temperature is beneficial to improve the interface properties of SiGe with the TiN/Y_2O_3 gate stack [3]. The TiN gate with PMA at 450°C can yield superior interface properties between Y_2O_3 and SiGe. In this work, we examine the impact of different gate electrodes on MOS characteristics of the Y_2O_3/SiGe gate stacks with different PMA temperature. Metal gates of Al, Au, W and TiN are used for this study.

2. Experiment

The process flow is shown in Fig. 1. 7-nm-thick non-doped $Si_{0.78}Ge_{0.22}$/p-type Si(100) wafers were cleaned by de-ionized water, acetone and diluted HF. Subsequently, 7-nm-thick Y_2O_3 was deposited at 300°C by ALD using $(CpMe)_3Y$ and H_2O. Then, 40-nm-thick TiN or W gate electrodes were deposited by metal sputtering, followed by 100-nm-thick Al gate contact. For comparison, 100-nm-thick Al or Au gate electrodes were also deposited by thermal evaporation. The metal gate of Al was patterned by NMD-3. W and TiN were patterned by APM. Au was patterned by a shadow mask. PMA was performed for 1 min at 300, 350, 400 and 450°C in N_2 ambient. D_{it} was extracted by the conductance method with considerations of surface potential fluctuation.

3. Results and Discussion

The C-V curves of Al, Au, W and TiN/Y_2O_3 gate stacks with PMA temperature optimized for D_{it}, which are 300, 300, 300, and 450°C, are shown in Fig 2. The large hysteresis of the Al/Y_2O_3 stack is attributed to diffusion of Al during PMA. We have confirmed the full degradation after PMA at 350°C [3]. The large frequency dispersion in the Au/Y_2O_3 under the accumulation condition stack may be caused by the series resistance from the back contact.

Minimum value of D_{it}, normalized C_{ox}, the hysteresis voltage and the leakage current of each metal on the Y_2O_3 stacks are shown in Fig 3 as a function of PMA temperature. It is found that the lowest D_{it} among all the gate stacks is obtained by the TiN gate stacks with PMA at 450 °C. The higher PMA temperature reduces both the hysteresis and the leakage current for metal gate except the Al gate. Unlike Au and W, C_{ox} of TiN/Y_2O_3 stacks reduces after PMA. This fact suggests that the composition or the thickness changes after annealing, which can contribute to the improvement in the gate stack properties.

4. Conclusions

We have studied the impact of metal gate electrodes on Y_2O_3/SiGe MOS interfacial properties with different PMA temperature. The TiN/Y_2O_3 gate stack with PMA at 450°C has been found to provide the best gate stack properties in comparison with Al, Au and W.

Acknowledgements

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References

[1] C.-H. Lee, et al., VLSI Symp., 2016, 36 [2] C.-T. Chang et al., IEDM, 2015, 584 [3] T.-E. Lee, et al., SISC, 2018, 212.

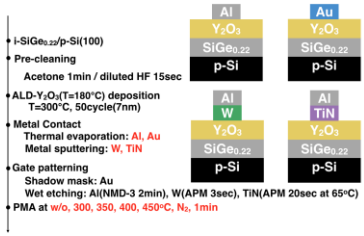

Fig.1: Process flow of Al, Au, W and TiN/Y_2O_3/SiGe MOSCAP.

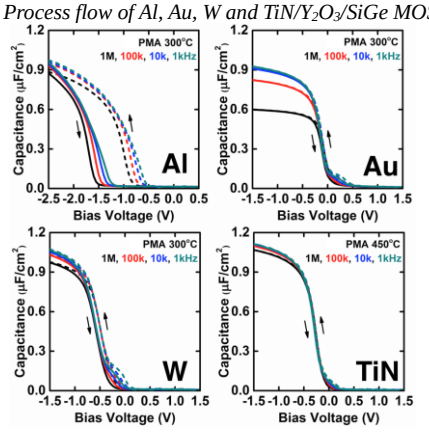

Fig.2: C-V curves of Al, Au, W and TiN/Y_2O_3/SiGe gate stacks with optimized PMA temperature.

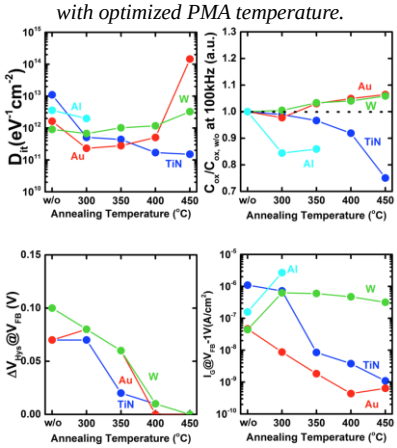

Fig.3: (a)D_{it} at E-E_i=-0.1eV (b)$C_{ox}/C_{ox,max}$ (c) ΔV_{hys} at V_{FB} (d) I_G at V_{FB}-1V with dependence of PMA temperature.