Sulfur vacancies degrade interface at valence band side in MoS_2 FET

○Nan Fang and Kosuke Nagashio
Department of Materials Engineering, The University of Tokyo
E-mail: nan@adam.t.u-tokyo.ac.jp

1. Introduction

Although stable *p*-type 2D-FET is required for complementary transistor operation, the transistor performance of defect-related *p*-type 2D channels, such as WSe_2, SnS_2 and so on, is generally low, compared with widely studied *n*-type MoS_2 FET [1,2]. Here, Nb doped *p*-type MoS_2 crystals are available now [3]. In this study, we study the hole transport of Nb-doped MoS_2 FET in order to reveal the interface states (D_{it}) at valance band (VB) side.

2. Transition from *p* to *n*-type

Fig. 1 shows I_D-V_{BG} curves for *p*-MoS_2 FET with different channel thickness on back-gate SiO_2/Si substrate. By decreasing the channel thickness, the transition from strong *p*-type to ambipolar and finally to *n*-type is reproducibly observed. For *p*-type behavior, the off-state is clearly found for the channel thickness of ~7nm, which indicates the maximum depletion width (W_{DM})[2]. Therefore, N_A can be estimated as ~ 2×10^{19} cm^{-3}, which is consistent with the previous Hall measurement[3].

The transition from strong *p*-type to *n*-type FET can be understood by "surface electron accumulation effect"[4]. Sulfur vacancies (V_S) is easily formed at "surface" in MoS_2 flake even during the fabrication process. Therefore, *n*-doping due to V_S is enhanced with reducing the channel thickness, especially for monolayer. Indeed, charge neutral point (CNP), as shown by arrow in **Fig. 1**, shifts negatively by decreasing the thickness. Although bulk doping density $N_A = \sim 2\times10^{19}$ cm^{-3} (equivalent to 7×10^{12} cm^{-2}) seems to be very high, it is still not enough to achieve *p*-type transport in nanoscale thickness device due to the surface V_S level of ~ 1×10^{13} cm^{-2}.

3. Origin for interface states at VB side

As shown in **Fig. 1**, on-current level is significantly reduced for *p*-side with decreasing the channel thickness, while it is still high for *n*-side even in monolayer. Since ohmic contact is observed for both polarities, these suggest that interface properties at VB side are more degraded than that at conduction band (CV) side. Therefore, the tetra-layer MoS_2/*h*-BN/graphite hetero-structure FET was fabricated to reveal whether interface properties at VB side are improved or not. I_D-V_{BG} curves in **Fig. 2** shows sub-threshold swing (*S.S.*) at current range (10^{-11}~10^{-12} A) for electron and hole are 160 and 590 mV/dec, relatively. I_D-V_{BG} curves are then fitted based on the accumulation-mode operation of MoS_2-FET [1,2]. Extracted D_{it} is shown in **Fig. 3(a)**.

According to our previous study for CB side[1,2], the main origin of D_{it} is the Mo-S bond bending due to the extrinsic issues, such as strain caused by high-*k* oxide deposition and/or the surface roughness of the SiO_2 surface. Therefore, D_{it} can be reduced by heterostructure formation, as observed here. On the other hand, as for VB side, D_{it} shows very high level over 10^{13} $cm^{-2}eV^{-1}$ even for 2D heterostructure device, which suggests that high D_{it} originates from MoS_2 itself, that is, V_S at the surface. As shown in **Fig. 3(b)**, V_S introduces shallow states at VB side, which spread widely by the interaction with valance band. Therefore, they act as strong trap sites. This is not the case for CB side since V_S states near the CB side are energetically quite sharp. Therefore, interface properties at VB side will be improved by the repairment of V_S [5].

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References [1] N. Fang *et al.,* J. Phys. D 2018, **51,** 065110. [2] N. Fang *et al.*, ACS Appl. Mater. Interfaces 2018, **10,** 32355. [3] J. Suh *et al.,* Nano let. 2014, **14,** 6976. [4] M. D. Siao *et al.*, Nat. Commun. 2018, **9,** 1442. [5] K.C. Santosh *et al.*, Nanotechnology, 2014, **25,** 375703.

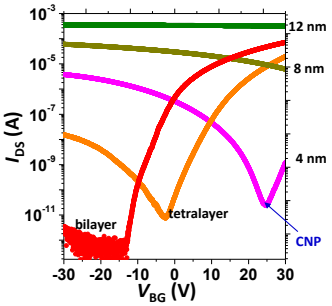

Fig. 1 I_{DS}-V_{BG} curves of Nb-doped MoS_2 FET on SiO_2/Si.

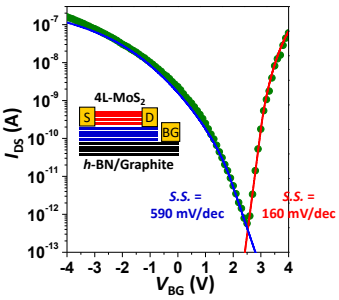

Fig. 2 Exp. and sim. of I_{DS}-V_{BG} curves of MoS_2/*h*-BN/graphite FET.

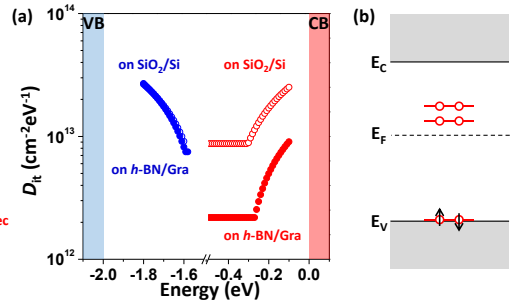

Fig. 3 (a) Extracted D_{it} of 4L-MoS_2 for both CB and VB sides. (b) Schematic of Vs induced defects levels.