Characterization and Modeling of FTJ Memristive Devices for in-Memory Computing

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Introduction

In the context of in-memory computing, emerging non-volatile memristive devices can be used as the memory computing element, storing learned features of incoming data while also performing computation at the location of the memory, drastically decreasing power consumption promoted by the intrinsic non-von-Neumann architecture of the system [1]. For successful adoption, memory elements employed in such circuits have a minimum set of requirements: nano-scale size, low-current operation, low device operation variability and analogue predictable switching under pulsing input [2].

Recently, analogue FTJ devices have received some attention as their gradual switching behavior is akin to memristive dynamics [3] and can offer promise in implementation as in-memory computing elements. Usually, FTJ devices exhibit binary switching, where the ferroelectric layer (FE) is maximally polarized in one direction to achieve binary operation [4][5]. However, under controlled pulsing, partial domains of the FE layer can be gradually switched and such allowing continuous modulation of the tunneling current across the device. Past efforts have shown partial characterization of CMOS-incompatible devices [3]. We present a pulsing study on HfSiO FTJ nano-scale memristive devices showing promising behavior suitable for novel in-memory computing systems.

Experimental

We characterized 24 devices with feature sizes of 150, 160, 180, 200, 300 and 500 nm [6]. Throughout our study, the device under test was measured at 3V after each applied pulse.

Our pulsing strategy involved an initial spot reading and *I-V* sweeping, followed by repeated pulsing with a maximum positive amplitude for our study (5V), followed by negative pulsing with same amplitude. The purpose is to find soft boundary G_{on} and G_{off} states which we then use in a subsequent pulsing algorithm which scans the conductance-pulse-amplitude (*G-V*) space to record the effect of several pulse amplitudes based on initial conductance state.

Fig. 1 shows an example measurement result of our *G-V* pulsing algorithm for a 200 nm FTJ memristor. Each marker represents relative conductance switch for one pulse with amplitude Vp (4µs) and initial conductance G_0. The device exhibits soft SET and hard RESET. Nonetheless, gradual conductance modulation is possible in both directions by using asymmetric voltage pulse amplitudes (higher for SET than RESET). We propose a behavioral model (not shown here) relating to positive (potentiating), and negative (depressing) relative conductance switch transitions, respectively. We test our fitted model against a pulsing run which also include random amplitude voltage pulses. The model is initialized with the start conductance state of the FTJ device and is updated based on received voltage pulse. The respective pulsing run is shown in Fig. 1 (left) showing excellent model agreement.

A simple application was demonstrated experimentally validating the analogue operation of FTJ memristive devices for in-memory computing systems [6].

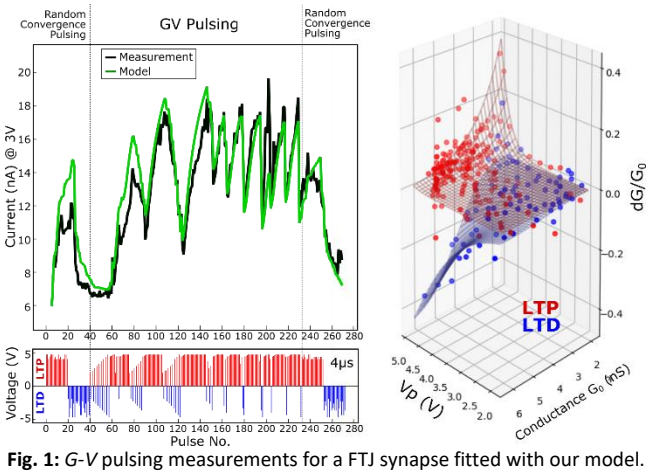

Fig. 1: *G-V* pulsing measurements for a FTJ synapse fitted with our model.

References

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