New routes and paradigms in Device Engineering for Nanoelectronics and Nanosystems

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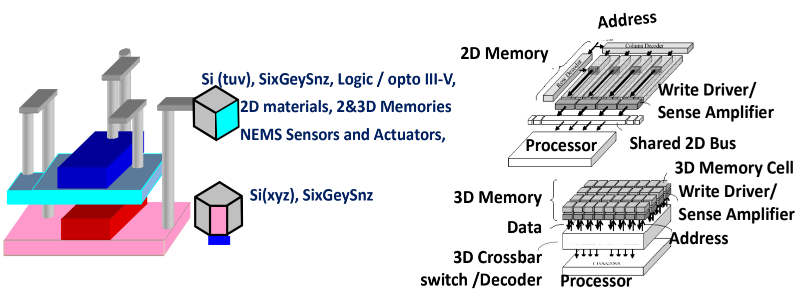
In the field of Nanoelectronics and Nanosystems, the down scaling of components has made possible the integration of more and more complex functions which can today be handheld. Nowadays, every human being on our planet is susceptible to own a mobile phone delivering access to information, services, leisure applications with multimodal communication. Challenges are ahead of us to meet the growing demand for Energy Efficient and Sustainable technologies not necessarily available with today's current schemes. In such a context, alternative devices and approaches are benchmarked for sensing, actuating, data storage and processing. They leave the floor to Integrated Intelligent Nanosystems[1,2] to match Low Power and High Performance either by Hybrid and Heterogeneous CMOS in 2D/3D(Fig. 1)[3] and give opportunities to Emerging Devices that will allow new computing schemes, such as complex quantum or neuromorphic computing[4,5]. In this frame, Thin films devices are the best candidates to face the drastic request of Energy and Variability Efficiency(E.V.E.) and Sustainability[4,5].

The evolution in the E.V.E. and Sustainability era already requests new technology integration paradigms appealing for new fabrication, characterization methods and tools involving actuation modes via mechanical, electron/particles, chemical, ion beams, photonic, magnetic interactions, … Such techniques are based on[2,4,5,6,7,8,9] : single ion implantation, molecular engineering and self-assembly, catalysis, Hydrogen/He ions implant or interactions, single or multi electron beam, molecular or single atomic sheet materials, …



(a) (b)

Figure 1 (a)Monolithic/Sequential 3D integration makes Heterogeneous co-integration of materials and sensors possible thanks to cold end processing at mid process: 50% improved area and energy delay product can be obtained on partitioned Si CMOS FPGAs. High density Embedded intelligence(sensors, actuators,…) is accessible; (b) High density or 3D memories (DRAM, RERAM) embedded with digital/analog circuits can deliver more bandwidth, reduce latency, introduce massively parallel «in-memory-immersed» neuromorphic and programmable or quantum computing architectures[2-5].

References

[1] "*Electronic Devices Architectures for the NANO-CMOS Era*", S.Deleonibus, Editor, Pan Stanford Publishing (Singapore), (2008).
[2] *Pan Stanford Series on Intelligent Integrated Nanosystems,* Simon Deleonibus, Editor, Pan Stanford Publishing (Singapore), vol. 1, (2014); vol. 2, (2017); vol. 3,(2018).
[3] P.Batude et al., Proc. IEDM 2017, pp. 52-55, San Francisco(CA), (2017)
[4] S. Deleonibus . IEEE Journal of the Electron Devices Society,(2016), vol. 4, n°5, pp.236-245Sept 2016
[5] S.Deleonibus et al., Proc. IEDM 2014, pp. 9.2.1 - 9.2.4, 10.1109/IEDM.2014.7047015, (2014)
[6] T.Shinada et al. (1998), J.Vac.Sci.Technology B,**16**, 2489-2493
[7] M.Bruel , Electronic Lett.,(1995), vol. 31, n°14, pp.1201-1202.
[8] S. Ogawa et al., Jap.Journ. Appl. Phys (**49**), (2010) , 04DB12
[9] M.E. Schmidt et al., ACS Appl. Mat. Interfaces, (2018), **10**, 10362-10368.