Vertical Triple-Ion-Implanted β-Ga_2O_3 MOSFETs with Nitrogen-Doped Current Blocker

National Institute of Information and Communications Technology[1], Tokyo University of Agriculture and Technology[2], Tamura Corporation[3]

°Man Hoi Wong[1], Ken Goto[2,3], Hisashi Murakami[2], Yoshinao Kumagai[2], Masataka Higashiwaki[1]

E-mail: mhwong@nict.go.jp

Vertical power switching devices are desirable for high-voltage applications since they allow for superior field termination, high current drives, and simplified thermal management. β-Ga_2O_3 (Ga_2O_3) is amenable to doping with both shallow donors (Si) [1] and deep acceptors (Mg, N) [2] by ion implantation with efficient dopant activation at a low thermal budget, thereby enabling device fabrication by a highly manufacturable all-ion-implanted process resembling that for SiC MOSFETs. In this work, a current aperture vertical Ga_2O_3 MOSFET is demonstrated by integrating N-ion (N^{++}) and Si-ion (Si^{+}) implantation doping [3].

The depletion-mode vertical Ga_2O_3 MOSFET consisted of a 5-µm-thick Si-doped (2.5×10^{16} cm^{-3}) n^{-}-Ga_2O_3 drift layer grown by halide vapor phase epitaxy (HVPE) [4] on an n^{+}-Ga_2O_3 (001) substrate (Fig. 1). A buried current blocking layer (CBL) for source–drain isolation was formed by N^{++} implantation doping. To recover implantation damage and activate N as a deep acceptor, thermal annealing was performed at 1100°C for 30 min in N_2 [2]. Subsequent Si^{+} implantations defined the electron channel and n^{++} source contacts that were activated at 950°C and 800°C, respectively, for 30 min in N_2. A 50-nm-thick Al_2O_3 gate dielectric was then grown by plasma-assisted atomic layer deposition. Ti/Au and Ti/Pt/Au were used for the ohmic and gate electrodes, respectively. Device fabrication was completed with the deposition of Ti/Au source probing pads on the Al_2O_3 for low pad leakage. The MOSFETs had an aperture opening of 20 µm and a gate length of 2.5 µm.

The vertical MOSFETs delivered a drain current density (I_D) of 0.42 kA/cm^2 (normalized to the Si channel implant area) and a corresponding specific on-resistance of 31.5 mΩ·cm^2 at a gate voltage (V_G) of +5 V (Fig. 2). A high I_D on/off ratio of over 10^8 was achieved, where the off-state I_D was dominated by gate leakage. The three-terminal off-state breakdown voltage of these devices was limited by Al_2O_3 breakdown to less than 30 V owing to the high Si doping over the aperture. Under 5-µs gate-pulsed conditions at a quiescent gate bias (V_{GQ}) of -40 V and a constant drain bias (V_D) of 20 V, the MOSFETs demonstrated potential for high speed switching operation by virtue of a large I_D when pulsed on, yet a small positive threshold voltage shift attributable to bulk or interface electron trapping under the gate was observed (Fig. 3). With improved dielectric quality and optimized doping schemes, this work promises a disruptive impact on Ga_2O_3-based power electronics.

This work was partially supported by Council for Science, Technology and Innovation (CSTI), Cross-ministerial Strategic Innovation Promotion Program (SIP), “Next-generation power electronics” (funding agency: NEDO).

[1] K. Sasaki *et al.*, Appl. Phys. Express **6**, 086502 (2013). [2] M. H. Wong *et al.*, Appl. Phys. Lett. **113**, 102103 (2018). [3] M. H. Wong *et al.*, IEEE Electron Device Lett. (2019), *in press*, doi: 10.1109/LED.2018.2884542. [4] K. Goto *et al.*, Thin Solid Films **666**, 182 (2018).

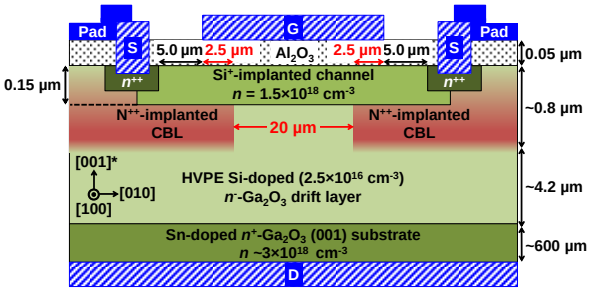

Fig. 1. Cross-sectional schematic of the vertical Ga_2O_3 MOSFET. The aperture and source widths were 200 µm.

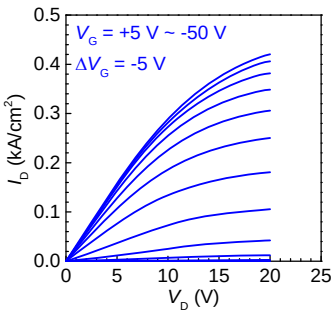

Fig. 2. DC output characteristics of the vertical MOSFET.

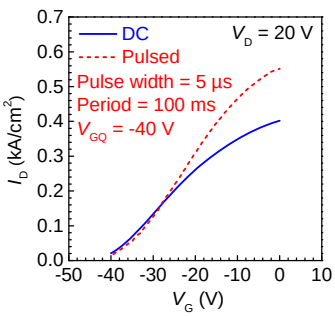

Fig. 3. DC and pulsed transfer curves of the vertical MOSFET.