β-Ga_2O_3 MOSFETs with Nitrogen-Ion-Implanted Back-Barrier

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β-Ga_2O_3 (Ga_2O_3) has recently captured significant attention as the next high performance power electronics material. Opportunities also exist for Ga_2O_3 transistors to operate as amplifiers capable of GHz switching speeds [1]. As the gate length of the devices decreases to allow for higher frequency of operation, improved confinement of the electron channel – typically achieved through a back-barrier with *p*-type doping or a wider bandgap – becomes critical for mitigating short-channel effects. This work capitalizes on the deep acceptor nature of nitrogen in Ga_2O_3 [2] for back-barrier doping in lateral Ga_2O_3 MOSFETs.

To accentuate the efficacy of the nitrogen-doped back-barrier, *n*-type conductive Ga_2O_3 was used as a base material for device fabrication (Fig. 1). Nitrogen was ion-implanted into the Si-doped Ga_2O_3, which was grown by halide vapor phase epitaxy (HVPE) [3], at an energy of 480 keV and a dose of 4×10^{13} cm^{-2}. Thermal annealing was carried out at 1100°C for 30 min in N_2 for lattice recovery and dopant activation [2]. Subsequent Si-ion (Si^+) implantations formed the electron channel (1.5×10^{18} cm^{-3}, 0.15-μm-thick box profile) and n^{++} contact layers (5×10^{19} cm^{-3}, 0.1-μm-thick box profile) that were activated at 950°C and 800°C, respectively, for 30 min in N_2. A 50-nm-thick Al_2O_3 gate dielectric was then formed by plasma-assisted atomic layer deposition. Ti/Au was used for the ohmic electrodes and pads, while Ti/Pt/Au was used for the gate electrode. Inter-device isolation was accomplished by the aforementioned nitrogen ion (N^{++}) implantation step without mesa etching. The MOSFETs had a gate length of 5 μm, a gate width of 200 μm, and source/drain access regions of 5 μm.

Circular transfer length method measurements revealed conductive source and channel implants over the back-barrier with sheet resistances of 420 and 9270 Ω/sq, respectively. Carrier depth profiling by 1-MHz capacitance–voltage measurements using on-chip MOS capacitors confirmed full Si activation in the channel. The MOSFETs delivered a maximum drain current density (I_D) of 103 mA/mm at a gate voltage (V_G) of +5 V (Fig. 2) and a peak transconductance (g_m) of 3.5 mS/mm at a drain voltage (V_D) of 20 V (Fig. 3). Given a low gate leakage current (I_G) of ~1 pA/mm, a minimal off-state I_D of 26 pA/mm resulted in a high on/off current ratio of 4×10^9 (Fig. 3), which attested to the efficacy of the N^{++}-implanted back-barrier in isolating the channel from the conductive buffer layer.

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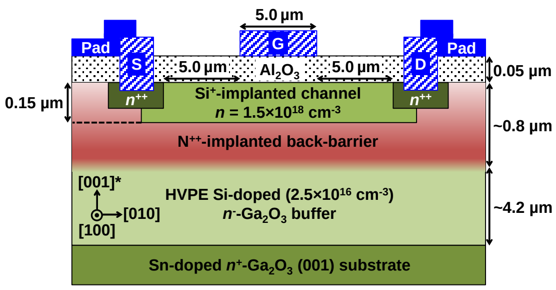

Fig. 1. Cross-sectional schematic of the Ga_2O_3 MOSFET.

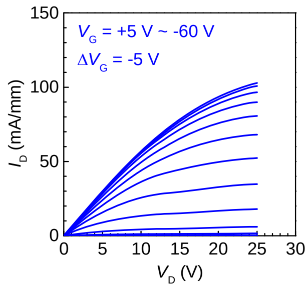

Fig. 2. DC output curves of the Ga_2O_3 MOSFET.

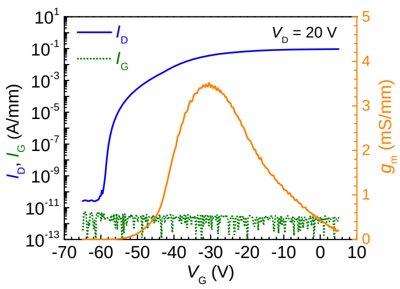

Fig. 3. DC transfer characteristics of the Ga_2O_3 MOSFET.