The spiking neural-network is an energy-saving computer capable of parallel-distributed processing, consisting of many cores, each including an arithmetic unit and memory as shown in Fig. 1. Memory in the cores store temporary states $x_j$ of neurons as well as synapse parameters $w_{ij}$, which indicate connectivity among neurons. The arithmetic unit performs mainly multiply-and-add calculations of $w_{ij}$ and $x_j$

$$h_i = \sum_j w_{ij} x_j.$$ (1)

Although static random access memory (SRAM) and a digital arithmetic unit are normally used in the core, energy-efficiency is expected to be much improved by employing magnetic technologies such as race-track memories and skyrmion tracks. Another method for energy-saving is the adoption of a core composed of an analog memory and arithmetic unit. To reduce the degradation of performance in analog-cores caused by scattering in the transistor characteristics, the authors introduce an analog memory cell in which a floating diffusion amplifier (FD Amp.) is included as shown in Fig. 2. The circuit has been used for the image cell in the CCD and CMOS sensors, in which charge induced in a photodiode is transformed to voltage using FD Amp. In this memory the photodiode is replaced by the capacitor formed by pn junction. The correlated double sampling circuits (CDS) can be used to suppress the fixed noises in the voltage signal.

![Fig. 1 Core includes memory and arithmetic unit.](image1.png)

![Fig. 2 Analog memory cell including FD amp.](image2.png)
