Steep Slope (<60mV/dec) and Hysteresis Characteristics in Junctionless SOI Transistors at Low Drain Voltage of 50mV

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[Introduction] Junctionless (JL) transistor, which has highly doped channel with same polarity of source/drain (S/D), can achieve steep SS<60mV/dec due to impact ionization (II) at lower drain voltage (V_D) compared to inversion-mode (IM) transistor due to its high II rate. However, relatively high V_D >1.6V is still required to trigger the II effect, which is too high for low power applications [1, 2]. In this work, we fabricated planar p-type JL transistors and observed steep SS less than 60mV/dec at low V_D of 50 mV, where the II is negligible. The origin of steep SS is discussed based on experimental results.

[Results and Discussion] Fig.1 shows the I_D-V_G curve of fabricated JL transistors. Apparently, steep SS is observed although clockwise hysteresis is also observed. There are two slopes in the forward sweep (SS_{F1} and SS_{F2}) while there is almost constant slope in backward sweep (SS_B). Fig.2 shows the dependence on the V_G scanning speed at V_D=-50mV. When the scan speed is very slow (0.007V/s), there is no hysteresis but SS is above 60mV/dec. As the scan speed becomes faster, hysteresis increases and SS decreases. Here, the hysteresis is divided into two components. Taking the slowest scan I_D-V_G without hysteresis as a reference, the V_{th} changes in forward and backward sweeps are defined as ΔV_F and ΔV_B, respectively. Fig.3 shows scan speed dependence of SS and hysteresis. Fig.4 shows the dependence on the V_G scan range at V_D=-50mV. Here, the lowest and highest V_G is defined as V_{GL} and V_{GH}, respectively. Only V_{GH} is varied in (a) and only V_{GL} is varied in (b). As shown in Fig.5, SS_{F1} and SS_{F2} depend on V_{GL} and SS_B and hysteresis depend on V_{GH}. Since steep SS is observed at V_D=-50mV, the cause of steep SS is not II. The measured results suggest that observed SS is caused by very slow response of I_D to V_G. When scan is fast, I_D cannot catch up and the response of I_D is delayed, resulting in hysteresis and steep SS. Fig.6 shows measured response of I_D to V_G in JL transistors, confirming the slow response. One of the possible origins may be the drift of mobile ions in the gate oxide [3].

[Conclusion] We observed steep SS below 60mV/dec in a p-type junctionless transistor. Steep SS is always accompanied hysteresis. It is speculated from V_G range and scan speed dependences that steep SS is caused by some transient phenomena with slow response.

[Reference] [1] R. Yu *et al.*, SSE, vol. 90, p. 28, 2013. [2] S.-M. Lee *et al.*, IEEE Trans. Electron Devices, vol. 60, p. 3856, 2013. [3] K. Endo *et al.*, SSDM, p. 217, 2018.

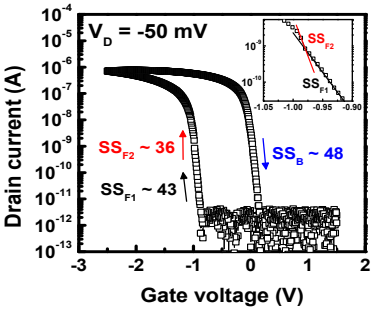

Fig.1: I_D-V_G curve of fabricated JL transistors. Scanning speed is 0.17V/s.

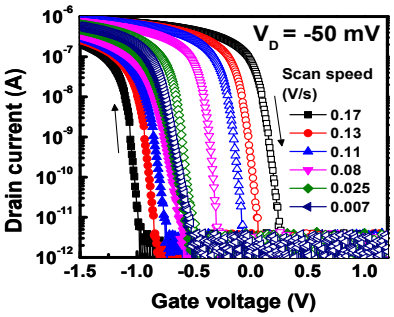

Fig. 2: Scan speed dependence of I_D-V_G. V_G is swept from 2 to -2.5 V.

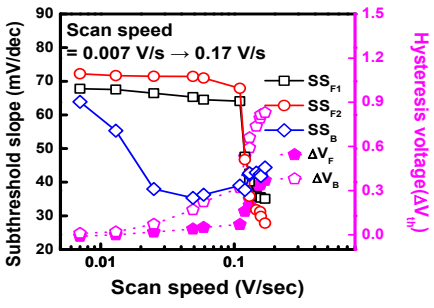

Fig. 3: Scan peed dependence of SS and hysteresis. V_D is -50 mV.

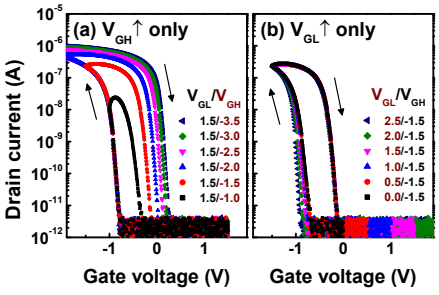

Fig.4: Dependence of I_D-V_G on sweep ranges. (a) Only V_{GH} is varied. (b) Only V_{GL} is varied.

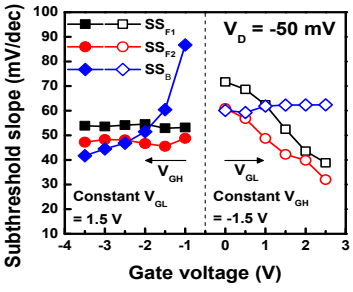

Fig. 5: Dependence of SS on V_{GL} and V_{GH}.

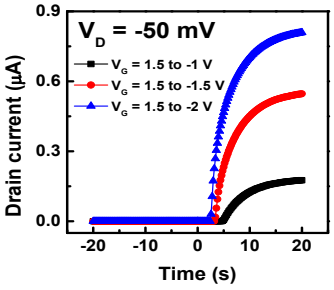

Fig. 6: Time responses of I_D to V_G change at t=0s.