Evolutional OPC as DTCO :
LWR and Sliming Effects on SNM of Fin-Trs SRAM by Computational Prediction

Kazuya Kadota, Nanoscience Lab., e-mail: drkadota@hotmail.co.jp

Recently high end semiconductors is going to advance to the sub 10 nm node after research and development and commercialization of the sub 20 nm node region.

In response to this need, lithography mask technology demands advancement and evolution of exposure techniques such as immersion exposure, inverse lithography and multi-beam mask writing. .

To realize that, it is necessary to overcome many problems from the viewpoint of device characteristics.

In particular, extremely severe problems have been accumulated in the formation of transistors, their single electronic characteristics, and integrated electronic characteristics from the viewpoint of lithography mask technology, and research and development is promoted intensively.

Specifically, the line edge roughness (LWR/LER) generated during the formation of the ultrafine transistor pattern is directly or indirectly influenced by resist material science, exposure light source and the like, and even in years of research and development, a clear solution has not been fulfilled.

In this study, a single Fin type transistor formed by immersion single exposure (SPT) of a sub 20 nm node, and computer simulation predicts how line edge roughness (LWR) occurring in the 6-Trs SRAM pattern adopting this method intentionally is applied on the computer and how it affects the device characteristics.

SRAM is widely adopted worldwide for high performance cache memories such as CPU and GPU, and the accuracy of the lithography / mask relation is required to be very strict specifications.
In addition, the Fin type is the mainstream for transistors that realize the SRAM of the sub 20 nm node with the highest accuracy and high reliability, and it is widely adopted for various products.
Furthermore, it is a promising transistor that will evolve into the future sub-10 nm node, and it is the object of research now. Figure 1 shows the overall flow of calculation prediction.

First, various 6Tr-SRAM cells are designed, and based on the data (gds), under simultaneous co-optimization (SMO) of light source and mask computer simulation of immersion lithography(Tachyon™) was carried out.

Intentionally, LWR was given on the optical image output (gds), and device simulation (HyENEXX) was then carried out to obtain the I-V and Static Noise Margin (SNM) of the entire SRAM cell.

Based on various thesis findings, LWRs given were sin curves of uniform frequency.

The results revealed that the LWR of about 3 nm or less has no influence on the operation characteristics such as SNM and I-V. (Figure 2)

With LWR of about 3 nm or more, it was predicted that SNM and I-V were greatly disturbed and it was impossible to form a device. At the same time it was found that Idint, which is a guideline for the operation speed of the SRAM, does not have a large influence even when the LWR is 4 nm.

On the other hand, as to the way of avoiding the generated LWR and reducing the influence, a resist slimming method can be considered as a corresponding process.

As for this measure, slimming treatment was deliberately carried out intentionally on the computer as well. As a result, if the slimming is about 2 nm or less, the device characteristics are not affected, but if the slimming is 2 nm or more, it can be calculated and predicted that the characteristics are greatly deteriorated.

As the result of this research, it was found that the line edge roughness (LWR) can be sufficiently evaluated by this computer prediction method, and the electronic characteristics prediction of the state-of-the-art SRAM and single transistor can be performed.

References:
K.Kadota et al., IEICE-1985, SPIE-922 (1988), SPIE-1088 (1989), PMJ-2011, PMJ-2013, PMJ-2016, MNC-2011, JSAP-2016, JSAP-2017, JSAP-2018, NGL-2017, NGL-2018

Acknowledgments: This research is part of the results of collaborative research with the National Institute of Advanced Industrial Science and Technology. The author expresses appreciation to all concerned parties.

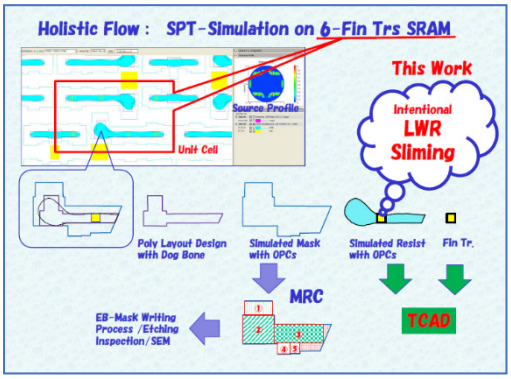
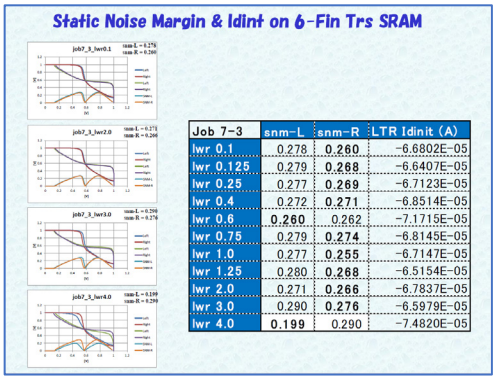


Fig.1 Holistic Flow:
SPT-Simulation on 6-Trs Fin-SRAM



Job 7-3	snm-L	snm-R	LTR Idinit (A)
lwr 0.1	0.278	0.260	-6.6802E-05
lwr 0.125	0.279	0.268	-6.6407E-05
lwr 0.25	0.277	0.269	-6.7123E-05
lwr 0.4	0.272	0.271	-6.8514E-05
lwr 0.6	0.260	0.262	-7.1715E-05
lwr 0.75	0.279	0.274	-6.8145E-05
lwr 1.0	0.277	0.255	-6.7147E-05
lwr 1.25	0.280	0.268	-6.5154E-05
lwr 2.0	0.271	0.266	-6.7837E-05
lwr 3.0	0.290	0.276	-6.5979E-05
lwr 4.0	0.199	0.290	-7.4820E-05

Fig.2 Static Noise Margin & Idint on 6-Fin Trs SRAM