# Reliability characteristics of Ferroelectric-$HfO_2$ capacitor with IGZO capping for 3D structure non-volatile memory application

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Recently, ferroelectric-$HfO_2$ FET memories have attracted more attentions [1], because of its good CMOS compatibility non-destructive readout, low power consumption and high program/erase speed. Toward even higher density, 3D vertical structure has been proposed. 3D vertical NAND type FeFET using Poly-si channel and its memory operation have been demonstrated [2]. However, there are several challenges with poly-Si channel such as low mobility of very thin poly-Si channel. IGZO is a promising channel material to solve these problems because its high mobility. IGZO FeFET also benefits from nearly-zero interfacial layer between IGZO channel and gate oxide [3]. However, the reliability characteristics of metal/FE-$HfO_2$/IGZO has not been fully investigated, yet.

In this paper, we fabricate and characterize the ferroelectric property of FE-$HfO_2$ with IGZO cap. Then, we investigate the impact of the IGZO cap on the reliability of the fabricated capacitor regarding endurance and retention characteristics. Lastly, an imprint effect on the capacitor is studied.

## Experimental results and discussion

First, we fabricated FE-$HfO_2$ capacitors. Fig. 1 shows the sectional and plane view of fabricated capacitor and the process flow. The ratio of $O_2$ is 3% for RTA. We characterize the ferroelectricity of the fabricated TiN/HZO/IGZO/Ti capacitor as shown in Fig. 2. Remanent polarization ($2P_r$) are from 19 $\mu C/cm^2$ to 30 $\mu C/cm^2$ in the sweep voltage range from 3V to 5V. Thanks to the low thermal expansion of IGZO, large $P_r$ is obtained [4].

Then, we characterize reliability of the TiN/HZO/IGZO/Ti capacitor. The fabricated capacitor realizes at least $10^8$ program/erase cycles before breakdown by mitigating the charge injection thanks to its nearly zero interfacial layer as shown in Fig. 3. In Fig.4 10-year retention is expected from the extrapolation. However, erase state has a worse retention characteristic because the depleted IGZO layer induces larger depolarization fields. Large asymmetric imprint is observed due to the asymmetric structure of fabricated capacitor. Fig. 5 (a) and (b) show the extracted shift of coercive voltage ($V_c$) in erase and program state. The horizontal shift after erase is relatively smaller than that after program. This is because the impact of the electron injection from TiN electrode with midgap workfunction is small due to high barrier height and the opposing electric field. On the other hand, the horizontal shift after program is larger than that after erase. This is because IGZO has wide band gap and small band offset to HZO, and the electron injection from IGZO is promoted. Finally, the $V_c$ shift caused by the imprint effect can be recovered by storing opposite state as shown in Fig. 6.

Reference: [1] J. Muller et al., VLSI Symp. 2012 [2] K. Florent, et al, IEDM 2018. [3] Fei Mo et al., VLSI, 2019. [4] R. Cao et al, IEEE EDL, 2018.

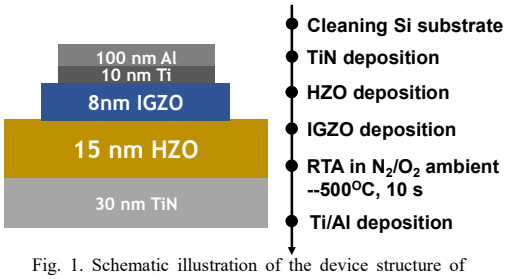


Fig. 1. Schematic illustration of the device structure of TiN/HZO/IGZO/Ti and the fabrication process flow.

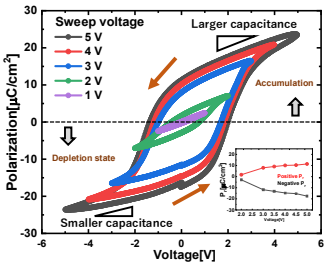


Fig. 2. P-V curves with different sweep voltage. Inset shows the $P_r$ versus sweep voltage.

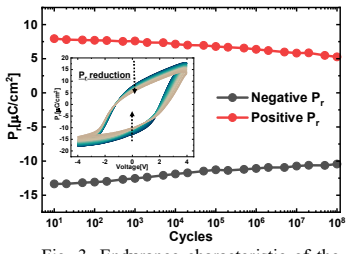


Fig. 3. Endurance characteristic of the fabricated capacitor. Up to $10^8$ cycles program/erase is achieved.

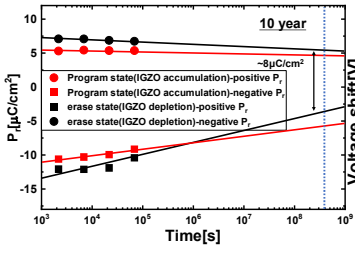


Fig. 4. Retention characteristics of the fabricated capacitor in program and erase state.

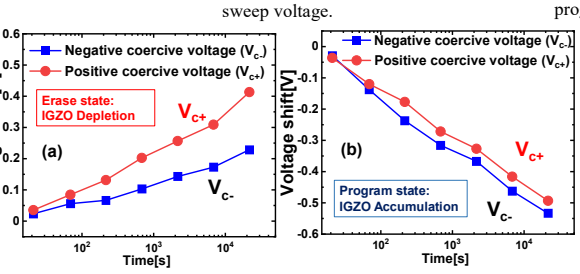


Fig. 5. Extracted shift of $V_c$ in erase (a) and program (b) state. Red and black show positive $V_c$ ($V_{c+}$) and negative $V_c$ ($V_{c-}$), respectively.

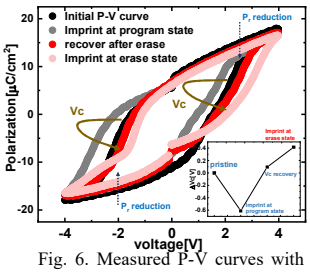


Fig. 6. Measured P-V curves with different device state. The inset is the extracted $V_c$.