GAA p-type poly-Si junctionless nanowire transistor with ideal subthreshold slope

Min-Ju Ahn, Takuya Saraya, Masaharu Kobayashi, and Toshiro Hiramoto
Institute of Industrial Science, University of Tokyo
E-mail: mjahn@nano.iis.u-tokyo.ac.jp

[Introduction] The adoption of gate-all-around (GAA) nanowire (NW) as a channel structure on the poly-Si transistor has demonstrated superior electrical performances thanks to its small-size volume with highly suppressed grain boundary (GB) defects as well as enhanced gate controllability [1]. Meanwhile, the concept of junctionless (JL) scheme has been attracted much attentions due to its simple process and volume conduction [2]. This JL scheme can be well matched with the GAA poly-Si nanowire transistor because they require small-size channel which strongly influences on subthreshold characteristics such as subthreshold slope (SS), threshold voltage (V_T) and off-current (I_{off}), which are key factors for low power applications. Among them, steep SS is the most powerful factor so that the theoretical limit of SS is highly desired. In this work, we fabricated GAA p-type poly-Si JL NW transistors, and observed ideal SS thanks to improved processes and suppressed GB defects.
[Experimental] The fabrication processes basically follow our previous work [3]. BF_2^+ ions, instead of B^+ ions, was implanted because BF_2^+ implanted device showed better SS and mobility than that by B^+ implantation due to the F passivation effect [4].The NW was defined by E-beam lithography and RIE, followed by wet-etching for suspending NW from the BOX. Fig.1 illustrates a 2D schematic, where the NW is connected to large S/D and extension regions. The extension regions operate as parasitic transistors. The L_{NW} and W_{NW} range from 250 to 1050nm and 5 to 20nm, respectively. The effective width (W_{eff}) is a perimeter of NW, and ranging from 20 to 50nm. The L_G is 30μm and height of NW (H_{NW}) is ~5nm. For comparison, a planar (PL) JL transistor with W/L=40/40μm was also fabricated. Fig.2 shows the top-view SEM image of the defined NW just after RIE.
[Results and Discussion] Fig.3 compares the normalized I_D-V_G curves of PL and NW transistor (W_{eff}=20nm, L_{NW}=250nm) at V_D=-0.05V. Obviously, the NW transistor shows steeper SS and enhanced current drivability. Inset shows the SS as a function of I_D×L/W. Extracted SS_{min} and SS_{ave} of NW transistor in the subthreshold region from I_D×L/W=1×10^{-12} to 1×10^{-9}A are 63 and 74mV/dec, respectively. The NW transistor shows excellent SS in a wide range of I_D. Fig.4 shows dependence of SS on W_{eff} and L_{NW}. The SS decreases with decreasing W_{eff}, which is reasonable because of reduced total GB defects in narrow NW. In contrast, SS slightly increases with decreasing L_{NW}. It is considered as the effect of parasitic transistors, not short channel effect because the L_G is long enough in our device shown in Fig.1. To remove the effects of parasitic transistors, substrate bias (V_{sub}) is applied. V_T of parasitic transistors with planar structure is shifted by body effect, while V_T of NW transistor is never changed owing to the GAA structure. In V_{sub}>0V, the parasitic becomes dominant, while I_D is governed by NW region in V_{sub}<0V [5]. As a results, actual NW characteristics can be obtained when V_{sub}<<0V. Fig.5 shows normalized I_D-V_{OV} (V_G-V_T) curves of NW transistor with V_{sub} of 0V and -25V. Notably, the SS and I_D of actual NW transistor are more improved by applying V_{sub} of -25V, especially SS_{min} and SS_{ave} are 60 and 62mV/dec.
[Conclusion] GAA p-type JL NW transistor with BF_2^+ implanted poly-Si was fabricated, and exhibits ideal SS with low I_{off}, which is attributed to improved processes and highly suppressed GB defects.
[Reference] [1] T. Y. Liu et al., IEEE EDL, 34, p.523, 2014. [2] J. P. Colinge et al., Nature Nanotech., 5, p.225, 2010. [3] M. J. Ahn et al., IEEE SNW, p. 53, 2020. [3] M. J. Ahn et al., IEEE SNW, p. 51, 2020. [4] M. J. Ahn et al., to be published in JJAP, 2020.

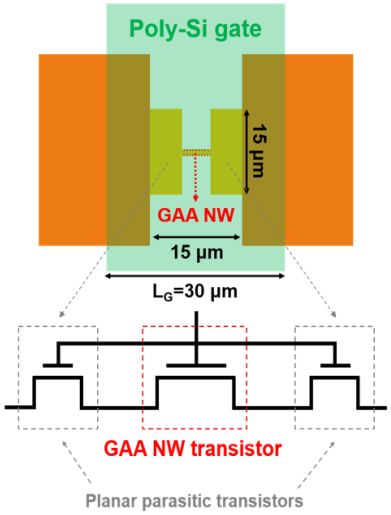

Fig.1: Schematics of top view of the GAA poly-Si JL NW transistor. The transistor includes parasitic components.

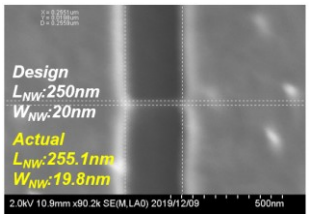

Fig.2: A top view of SEM image

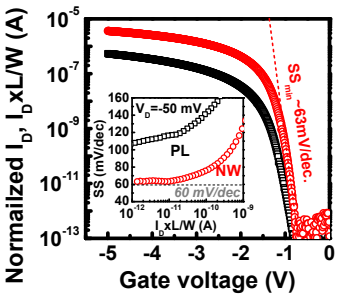

Fig.3: Normalized I_D-V_G curves of PL and NW transistors at V_D=-0.05. Inset is SS curves.

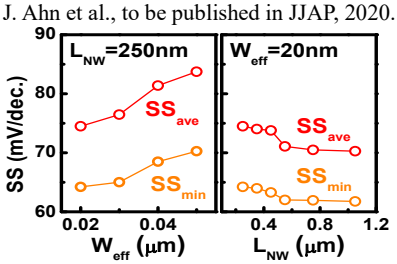

Fig.4: SS_{ave} and SS_{min} on W_{eff} and L_{NW}

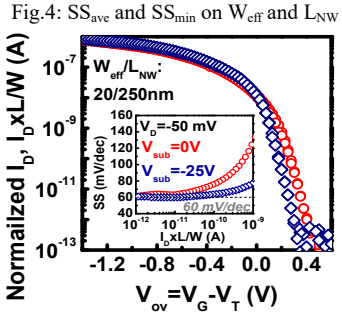

Fig.5: I_D-V_{OV} curves of NW transistors at V_{sub}=0, -25V. Inset is SS curves.