The Si-terminated 2DHG Diamond MOSFETs with the Normally-off operation and Wide Temperature Range Stability

Diamond exhibits excellent electrical properties such as high thermal conductivity about 22 kW m$^{-1}$K$^{-1}$, high breakdown field over 10$^7$ V/cm, and high bulk hole mobility of 2000 cm$^2$Vs$^{-1}$. We have developed the H-terminated (C-H) diamond MOSFETs by using the two-dimensional hole gas (2DHG) [1-2]. On the other hand, the electronegativity of Si is 0.7 Pauling unit lower than that of C, the different electronegativity (C: 2.5, Si: 1.8) C-Si dipole could more holes accumulate on the silicon termination diamond than the C-H (C: 2.5, H: 2.1) [3], the spontaneous polarization of C-Si dipole expects to induce the 2DHG which can used as the p-channel to fabricate the MOSFETs, and the SiO$_2$ also is advantageous for power devices in terms of chemical stability and wide band gap. The SiO$_2$ can be used as the gate insulator in the diamond power devices [4]. In this work, Si-terminated (C-Si) diamond MOSFETs has been fabricated with the boron-doped p$^+$ diamond selective growth by using the SiO$_2$ as the mask for source and drain formation and the gate insulator and the C-Si diamond MOSFET achieved Normally-off operations and wide temperature range stability.

High-pressure high-temperature (HPHT) Ib (001) diamond substrate has been used to fabricate the Si-terminated MOSFET (Fig.1) in this work, 260 nm SiO$_2$ layers was formed by utilizing TEOS-CVD, the conformation of the C-Si diamond surface was formed during the Boron-doped diamond selective growth by the MPCVD with the high temperature 727°C and hydrogen plasma (microwave output power 360W). The Ti/Pt/Au metal electrodes for source/drain and 100nm ALD Al$_2$O$_3$ layer for passivation was deposited, and the 100nm Al overlapping gate has been formed in this MOSFET. The electrical characteristics of this C-Si diamond MOSFET in the room temperature (300 K) and the high temperature (673 K) were shown in Fig.2. The obtained maximum drain current density of the C-Si diamond MOSFET (normalized by gate width 25um) is -118mA/mm at V$_{DS}$ = -30V and V$_{GS}$ = -40 V, the maximum gm is 2.43 mS/mm at V$_{DS}$ = -10 V, the field effect mobility ($\mu$$_{EF}$) is 111cm$^2$V$^{-1}$s$^{-1}$, and the threshold voltage is V$_{TH}$=-4.0V (achieving normally-off operation in the room temperature). For the high temperature operation, the maximum drain current density is increased to -125mA/mm, $\mu$$_{EF}$ reaches up to 190cm$^2$V$^{-1}$s$^{-1}$ and the threshold voltage still keeps the normally-off operation (V$_{TH}$=-2.8V). As a result, The C-Si MOSFET shows the excellent temperature stability and normally-off operation which will contribute significantly to the diamond p-FET for the complementary inverter circuits combined with GaN or SiC n-FETs.