MOS 構造での酸化物ゲート厚さのばらつきと界面準位密度の関連性の考察

Consideration of relationship between the variation of Gate Oxide Thicknesses and the density of interface states for MOS structure

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P-channel metal-oxide-semiconductor field effect transistors (p-MOSFET), also called pMOS, are fabricated by an advanced semiconductor fab: Minimal Fab [1,2]. Minimal Fab is characterized by a modern, cost-effective, fabrication concept [2]. The silicon wafers are minimized to a diameter of 12.5 mm and encapsulated in a shuttle to avoid any contamination, keeping white room condition during the full fabrication process, without the space and budget of a mega fab [2].

Here, the density of interface state (D_{it}) is monitored as a function of the oxide gate thickness (T_{ox}) to improve the yield of pMOS devices. The coupled D_{it} - T_{ox} variable can improve the reliability of pMOS characterization by underlining the interface Si-SiO_2 quality, which is associated to electrical performance by D_{it}. For this, we focused on the RCA chemical cleaning, prior to the gate oxide deposition, realized in three different Minimal Fab stations (RCA #4, #6, and #7) with specific final RCA step HCl/H_2O_2/DIW ratio: 1/1/100 and 1/1/6. The gate oxide deposition is then performed at 1150 ºC for 50 min by focused light heating. D_{it} is calculated about 10^{10} eV^{-1} cm^{-2} to 3×10^{11} eV^{-1} cm^{-2} from capacitance-voltage measurement at high and quasi-static frequencies [3], and T_{ox} is estimated between 67 nm to 74.5 nm from the maximum capacitance oxide. Figure 1 underlines that D_{it} - T_{ox} can give a precise “identity” of a specific RCA process, and underline possible interface damage due to plasma etching where D_{it} about 3×10^{11} eV^{-1} cm^{-2} is observed. An excellent interface quality is obtained with $D_{it} < 5\times10^{10}$ eV^{-1} cm^{-2}.

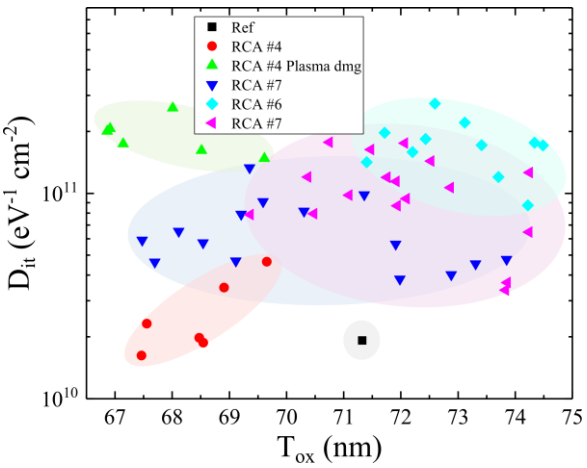

Figure 1: Interface state density (D_{it}) as a function of the oxide gate thickness (T_{ox}) with different RCA chemical cleaning prior to the gate oxide deposition.

References: [1] S. Hara et al., *J. Jpn. Soc. Precis. Eng.* **77** (2011) 249-253. [2] S. Khumpuang et al., *IEEE Trans. Semic. Manuf.* **28** (2015) 393-398. [3] A. V. Penumatcha et al., *IEEE Trans. Elec. Dev.* **60** (2013) 923-926.