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Power delay analysis of half and full adder circuits using GAA CNTFET with different chirality and channel

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Abstract: This work describes the analysis of half-adder and full-adder circuits using GAA-CNTFET which is basic element for digital circuits. As scaling down of transistors have become the major concern these days, it has led to the problems such as short channel effects (SCEs), leakage current, high power consumption. To deal with these problems, CNTFETs are used which have proved itself as a promising device in the world of electronics. The property called as “Ballistic Transport” made it even popular as it led to the highly efficient conductivity of the current in the device. It is also regarded as the best replacement for MOSFETs. The transient analysis, power analysis, delay measurement calculations is carried out in this work for full adder and half adder for different chiralities with different channels. Results shows that combination of Single Chirality Double Channel (SCDC) and Double Chirality Double Channel (DCDC) gives the efficient PDP in terms of performance of the circuit designed.

Keywords: Gate-All-Around Carbon Nanotube Field Effect Transistors (GAA-CNTFETs), MOSFET, half-adder, Full-adder.

CNTFET: The Moore’s law states that the transistor size in the integrated chip scales down by the factor of two for every two years. Scaling down of transistors leads to the Short Channel Effects (SCE), passive power consumption, electron tunneling through short channels. These limitations are eliminated by using Carbon Nanotube FETs. The structure of CNTFET is typically similar to that of MOSFET. CNTFET is beneficial over the conventional MOSFET in term of better control over the channel, reduction in carrier tunneling, short channel effects, reduced leakage currents, higher current density, and enhanced carrier velocity.

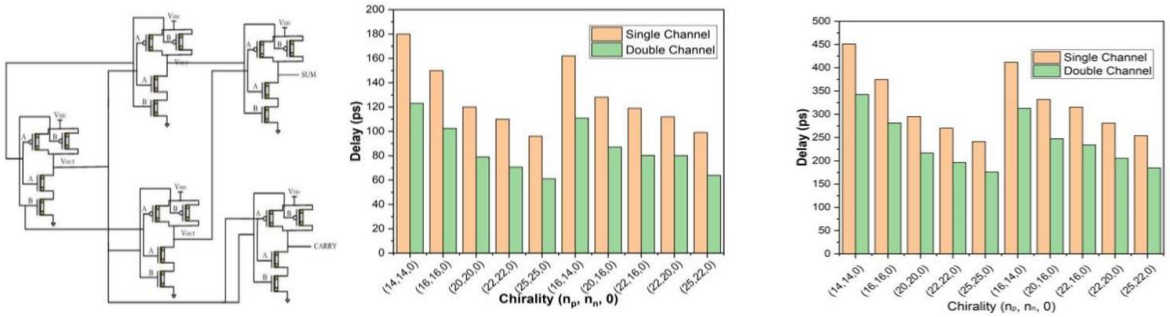

Figure (a) shows the circuit diagram implemetation of half adder using the GAA CNTFET. (b) Delay with different chirality for half adder (c) Delay with different chirality for full adder

Conclusion: Four types of configuration is implementated such as SCSC, SCDC, DCSC, DCDC for both half and full adder circuits. The result interpretation shows that there is a significant trade-off between power consumption and delay in CNTFET which is found based on the performance of adders built using GAA-CNTFETs. Results shows better power delay product efficency for SCDC and DCDC.

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