シリコンナノピラー/ナノワイヤの酸化メカニズム

Oxidation mechanism of Si nanopillar/nanowire

東北大学，○葉 術軍、山部紀久夫、遠藤哲郎

Tohoku Univ., ○Ye Shujun, Yamabe Kikuo, Endoh Tetsuo

E-mail: yeshujun@cies.tohoku.ac.jp

Vertical Gate-All-Around (GAA) is predicted to be the main structure of metal-oxide-semiconductor field-effect-transistor (MOSFET) beyond Moore. Variance of 1x-nm-diameter or smaller device fabricated by the current semiconducting process is a crucial issue for large-scale integrated circuits. We previously fabricated uniform sub-20-nm Si nanopillar arrays with a reduced diameter variance (to ±0.5 nm) and a cylindrical shape [1], which can be used for vertical GAA-MOSFETs, through controlling of oxidation of an array of tapered Si nanopillars [2-4] fabricated by an argon fluoride lithography followed by dry etching. It is necessary to design Si nanopillar arrays with a certain size and shape for fabrication of vertical GAA-MOSFET for practical applications, which requires the deeply understanding of oxidation of Si nanopillar. In this work, we analysis the stresses (oxidation-induced stress, compressive stress from both the old oxide and new oxide, tensile stress…) during the oxidation process as shown in Figure 1 and interpret the mechanism of oxidation of Si nanopillar.

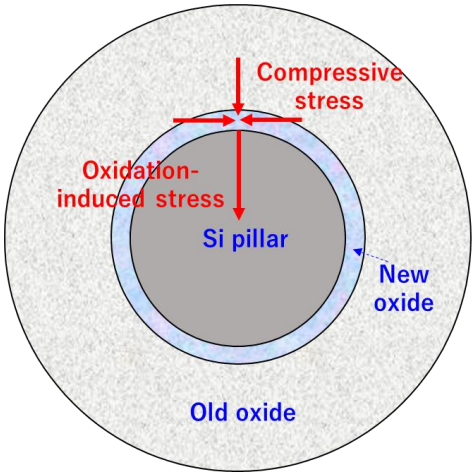

Figure 1　Schematic diagram of stress during the oxidation of Si nanopillar

(**This work is supported by the SIP, Cabinet Office, Government of Japan**)

[1] Ye S, Yamabe K, and Endoh T. *ACS Omega.* 4, **2019**, 21115.

[2] Ye S, Yamabe K, and Endoh T. *Materials Letters.* 258, **2020**, 126780.

[3] Ye S, Yamabe K, and Endoh T. *Journal of Materials Science.* 54, **2019**, 11117.

[4] Ye S, and Endoh T. *Materials Science in Semiconductor Processing.* 93, **2019**, 266.