

## Comparison of non-volatile memory characteristics for Hf-based MONOS diode with HfO<sub>2</sub> and HfON tunneling layer

Tokyo Institute of Technology, <sup>o</sup>Jooyoung Pyo, Yusuke Horiuchi, and Shun-ichiro Ohmi

E-mail: pyo.j.aa@m.titech.ac.jp, ohmi@ee.e.titech.ac.jp

### 1. Introduction

We have investigated Hf-based MONOS non-volatile memories (NVM) to improve the memory characteristics. The 6 V/2 ms operation was confirmed for the Hf-based MONOS NVM with HfO<sub>2</sub> tunneling layer (TL) [1]. However, SiO<sub>2</sub> interfacial layer (IL) between the TL and Si substrate would be formed which increases the equivalent oxide thickness (EOT) and degrades memory characteristics [2].

In this experiment, we utilized HfON as the TL of MONOS diodes to decrease the EOT and improve the memory characteristics [2].

### 2. Experimental procedure

After 100 nm SiO<sub>2</sub> growth and active area formation on p-Si(100) substrate, the HfO<sub>2</sub> or HfON TL (3 nm) was formed followed by in-situ deposition of HfN<sub>0.5</sub> (Gate; G, 10 nm)/HfO<sub>2</sub> (Blocking layer; BL, 8 nm)/HfN<sub>1.1</sub> (Charge trapping layer; CTL, 3 nm) by ECR plasma sputtering at room temperature [1-3]. The HfON TL was formed by the Ar/O<sub>2</sub> plasma oxidation of 2 nm-thick HfN [3]. Then, post-deposition annealing was carried out at 600°C/1 min in N<sub>2</sub>. After the Al electrode was evaporated and patterned to form a contact electrode, the HfN<sub>0.5</sub> metal layer was etched by DHF. Then, Al back electrode was evaporated. The electrode size was 100 × 100 μm<sup>2</sup>. The fabricated samples were characterized by C-V measurements.

### 3. Results and Discussion

Figure 1 showed the flat-band voltage shift depends on the pulse width and voltage characteristics of MONOS NVM diodes. The measured EOT of HfO<sub>2</sub> and HfON TL MONOS NVM diodes was 7.2 and 4.9 nm and the memory window (MW) was obtained as 2.9 and 3.5 V at the program/erase (P/E) condition of ±8 V/100 ms, respectively. The HfON TL operated below the HfO<sub>2</sub> TL P/E condition of 6 V/2 ms [1]. The HfON TL obtained 0.8 V of MW even for low P/E conditions, such as ±5 V/100 μs. This is because the SiO<sub>2</sub> generation at the interface was suppressed [2]. Therefore, the EOT and P/E condition of HfON TL MONOS NVM diode was improved than HfO<sub>2</sub> TL.

### 4. Conclusion

In this paper, the effect of HfON TL of MONOS

NVM diode was investigated to improve the memory characteristics. Because of the decreased EOT and suppression of the SiO<sub>2</sub> IL formation, the HfON TL operated at the ±5 V/100 μs of P/E condition which is faster than HfO<sub>2</sub> TL.

### Acknowledgement

The authors would like to thank Mr. M. Suzuki of Tokyo Institute of Technology, the late Prof. Emeritus T. Ohmi, Prof. T. Goto, Prof. R. Kuroda and Prof. T. Suwa of Tohoku University, Dr. M. Shimida and Mr. M. Hirohara of JSW-AFTY for their support and helpful discussion on this research. This work was partially supported by JSPS KAKENHI Grant Number 19H00758 and Toshiba Electronic Devices & Storage Corporation.

### Reference

- [1] S. Kudoh et al., 2017 SSDM, pp. 24-25 (2017).
- [2] J. Pyo et al., IEICE Tech. Rep. **119**, pp. 21-24 (2019).
- [3] D. H. Han et al., IEICE Electron. Exp. **10**, 20130651 (2013).

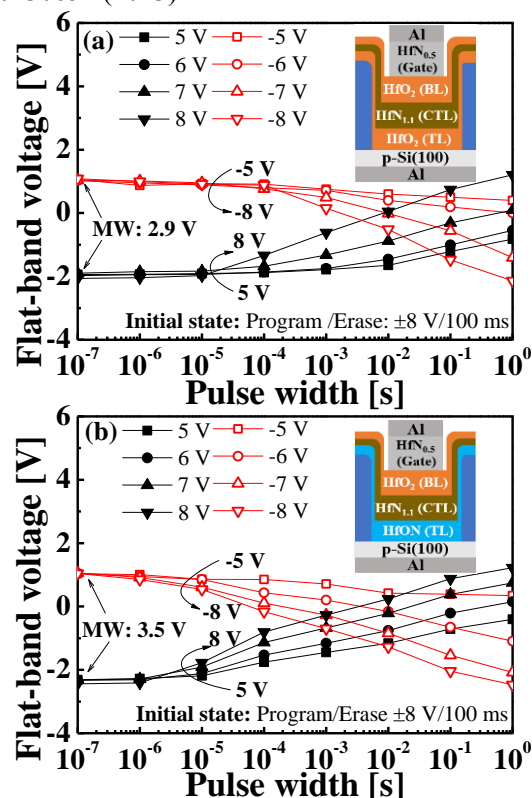


Figure 1. Dependence of the pulse width and voltage characteristics of (a) HfO<sub>2</sub> and (b) HfON TL MONOS diode.