Influence of Interface Traps on Split *C-V* Characteristics of 4H-SiC MOSFETs

Univ. Tsukuba, ◦(D)Xiaoran Cui, Dai Okamoto, Noriyuki Iwamuro, and Hiroshi Yano
E-mail: s1836007@s.tsukuba.ac.jp

1. Introduction

SiC is one of the most promising wide-bandgap semiconductors for power devices. However, the high density of interface states (D_{it}) in 4H-SiC/SiO_2 structures leads to the poor properties of 4H-SiC MOSFETs [1]. N-type SiC MOS capacitors are usually utilized to estimate n-channel SiC MOSFET performance, because D_{it} measurement using the MOS structure is only possible on the majority carrier side due to the wide bandgap of SiC. However, the differences in the dopant elements of *n*-type and *p*-type substrates may affect the SiO_2/SiC interface properties, so the D_{it} near E_C should be evaluated from measurement performed on n-channel 4H-SiC MOSFETs with *p*-type layer. In this work, the split *C-V* technique was applied on n-channel 4H-SiC MOSFETs to acquire C_{GC}-*V* and G_{GC}-*V* curves for investigation of interface traps in 4H-SiC/SiO_2 structures, though this technique is usually adapted to mobility evaluation.

2. Experiments

Quasi-static and high-frequency split *C-V* measurements were both performed on n-channel 4H-SiC MOSFETs with gate voltage range between -10 V and 20 V. The gate oxides (t_{ox} = 50 nm) of the sample were formed by dry oxidation followed by nitridation for 10 min. The equivalent measurement circuit is shown as inset (left side) in Fig. 1 [2].

3. Results and Discussion

Fig. 1 shows C_{GC}-*V* curves with different frequencies. In Fig. 1, there is a "ledge" (enlarged view of the "ledge" is shown as inset in Fig.1) as gate voltage is about 3.5 V. Fig. 1 also indicates that the "ledge" shape is dependent on frequency. It can be seen that the "ledge" disappeared when measured at 1 Hz. This can be explained as when the frequency of the AC gate voltage is too low like 1 Hz, all interface traps immediately change occupancy in response to the AC gate voltage. So the C_{GC}-*V* curve becomes smooth. As frequency increases to a very large value like 100 kHz, interface trap occupancy seldom changes in response to the AC gate voltage, so the "ledge" becomes not as steep as the 10 kHz C_{GC}-*V* curve. The frequency dependency of "ledge" shape implies the "ledge" is caused by interface traps near E_C.

Fig. 2 shows the C_{GC}-*V* and G_{GC}-*V* curves with frequency of 1 kHz. The peak, which is circled on G_{GC}-*V* curve in Fig. 2, appears at the same voltage (about 3.5 V) when the "ledge" appears on C_{GC}-*V* curve. This peak on the G_{GC}-*V* curve implies that there is an energy loss caused by interface traps near E_C. At DC gate voltage is lower than 3 V or higher than 4 V, interface traps do not respond with the AC gate voltage, thus the energy loss decreases.

Height of the "ledge" is defined as the height from point A (red dot) to point B (green dot), which is shown in Fig. 2 as an inset. The height of "ledge" means the capacitance caused by interface trap, and with a larger channel length, the height of "ledge" increases linearly.

4. Conclusion

Split *C-V* technique was applied on n-channel 4H-SiC MOSFETs to characterize interface properties of SiO_2/SiC structures. The mechanism of the "ledge" and peak shapes in the C_{GC}-*V* and G_{GC}-*V* curves were explained by interface traps.

Acknowledgement

This work was supported in part by JSPS KAKENHI Grant Number JP16H04326.

References

[1] T. Hatakeyama *et al*,Appl. Phys. Express 10,046601 (2017)
[2] D.K. Schroder, Semiconductor Material and Device Characterization (Wiley, Arizona State, 2006)

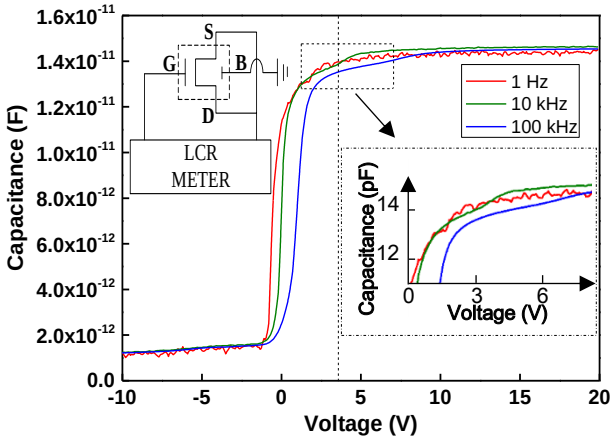

Fig. 1. C_{GC}-*V* curve of NO10 sample.

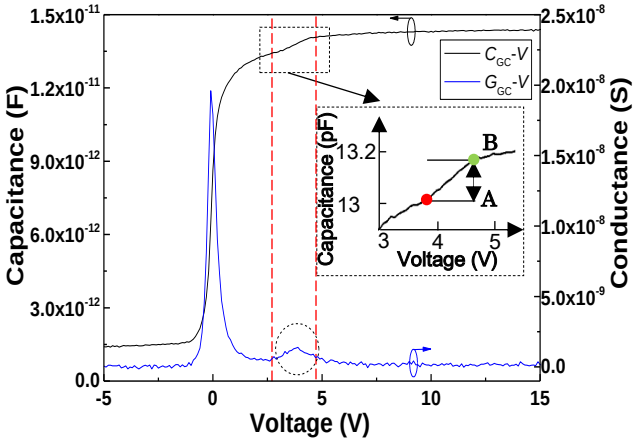

Fig. 2. C_{GC}-*V* and *G-V* curve of NO10 sample at 1 kHz