## High quality AlN film on sapphire prepared by two step sputtering-annealing

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High quality and low cost AlN substrates are important for both ultra-violet light emitting diodes (UV-LEDs) and electronic devices. Previously, we have realized high quality AlN/sapphire templates by face-to-face annealing of sputter-deposited AlN on sapphire, with threading dislocation density (TDD) as low as  $2 \times 10^8$  cm<sup>-2</sup>.<sup>[1,2]</sup> To further reduce the TDD, longer annealing time and thicker AlN film are required for sufficient dislocation annihilation. However, with increasing annealing time and AlN film thickness, imperfections like pits will generate on the AlN surface. In this work, we demonstrate high-quality AlN on sapphire with TDD as low as  $4 \times 10^7$  cm<sup>-2</sup> prepared by two sputtering-annealing steps. Using a second sputter-annealing on top of a sputter-annealing prepared AlN thin film instead of one-step sputtering, the AlN layer is able to undergo a longer annealing time with almost no pits, resulting in a TDD of  $4 \times 10^7$  cm<sup>-2</sup> after annealing at 1725 °C for 9 hours, estimated by X-ray rocking curves (XRC) measurements in Fig.1. The high-quality AlN templates are expected to breed high-performance nitride-based UV-LEDs and electronic devices.



Fig 1. (a) XRC measurement results of a 1.2-µm-thick AlN prepared by two step sputtering-annealing after annealing at 1725 °C for 9 hours. (b) Dislocation densities with different annealing time for AlN prepared by two step sputtering-annealing.

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[2] K. Uesugi, et al., Appl. Phys. Express 12, 065501 (2019).

<sup>[1]</sup> H. Miyake, et al., J. Crystal Growth 456, 155 (2016).