Fabrication of Vertical Aligned Germanium Nanowires by Nanoimprint Lithography

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Introduction

Ge has a lower carrier effective mass (electrons and holes), thus higher charge carrier mobility than Si. Its excellent electronic transport properties make it a prime candidate material for fabricating next-generation Si-compatible electronic and optoelectronic devices. Vertical Ge nanowire arrays are of particular interest due to their large surface to volume ratio and high integration that has been proposed to be an ideal material for a high-speed vertical gate-all-around field-effect transistor (FET). On the other hand, nanoimprint lithography (NIL) and Bosch process have been widely used to achieve Si nanowire array with small diameter and high aspect ratio [1]. However, there are few reports on the top-down fabrication of Ge nanowire array.

This study's aim is to develop a method to fabricate uniform Ge nanowire arrays with a smooth surface by nanoimprint lithography and Bosch process.

Experimental section

The fabrication steps of germanium nanowire arrays are shown in Figure 1. First, p-Ge(100) substrates were patterned by a 30-nm-thick MgO layer by UV-NIL and lift-off processes Then, SF_6 plasma followed by C_4F_8 plasma (Bosch process) was applied for deep etching of Ge nanowire structure. The flow rates of SF_6 and C_4F_8 were both fixed at 35 sccm with a chamber pressure of 0.75 Pa and an RF power of 100W. To reduce the diameter of the nanowire, the samples were treated with H_2O_2 (3%) solution at room temperature for 0 to 240 s. Then, the morphology of nanowires was studied using scanning electron microscopy (SEM).

Results and discussion

Figure 2a shows the successful fabrication of Ge nanowire arrays with an orderly arrangement. 25 cycles of the Bosch process results in the nanowire arrays with a diameter of 200 nm and a height of 800 nm shown. The pitch size of the nanowire arrays is determined by the imprint mold used in the NIL process. The inset in Figure 2a shows the sidewalls are vertical and smooth. Figure 2b shows the morphology of Ge nanowires after etching by H_2O_2 solution for 240 s. The diameter of the nanowire was decreased from 200 nm to 30 nm and the surface roughness was also reduced.

[1] Morton, Keith J., et al. Nanotechnology 19.34 (2008): 345301.

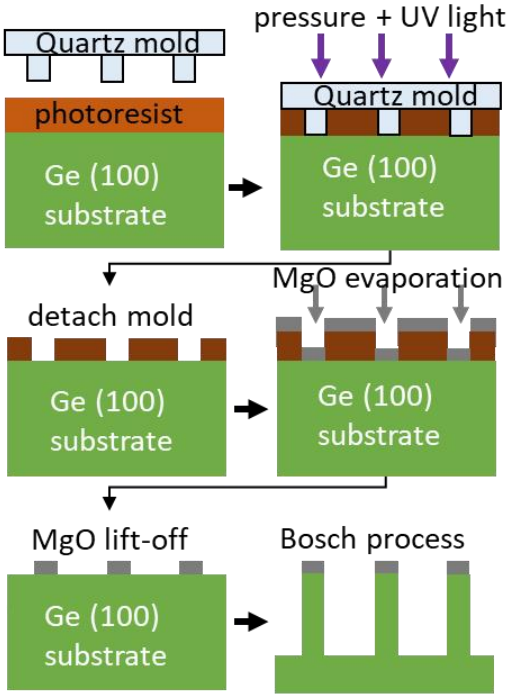

Figure 1. Schematic of top-down fabrication of Ge nanowire arrays.

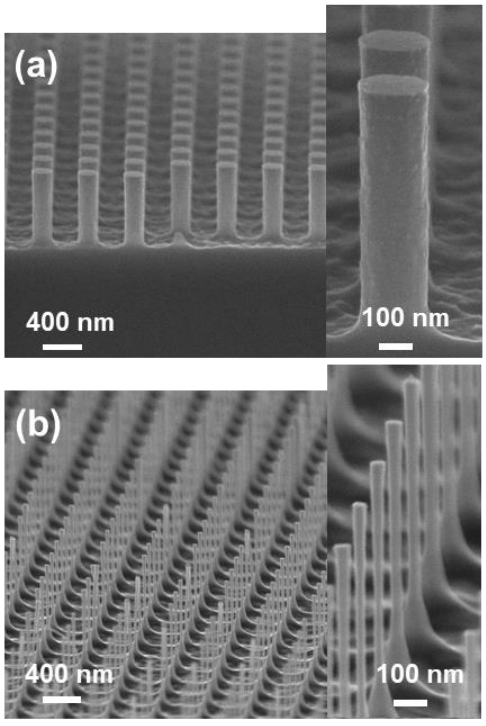

Figure 2. 15° tilted cross-sectional SEM images of Ge nanowire arrays before (a) and after (b) H_2O_2 etching .