Improvement of ferroelectric properties of TiN/$Hf_{0.5}Zr_{0.5}O_2$/Si gate stacks by inserting Al_2O_3 interfacial layers

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Introduction The HfO_2-based ferroelectric field-effect-transistor (FeFET) has attracted a significant interest because of its scalability and CMOS process compatibility for possible applications such as memory and neuromorphic computing [1, 2]. Here, the interfacial layer (IL) plays a critical role in the FeFET performance. Formation of the ferroelectric o-phase in doped HfO_2 is largely dependent on the boundary conditions provided by IL [3]. In addition, scaling the thickness of IL is crucial for achieving low voltage operation [4]. Moreover, the inversion charge density [5] of FeFETs is much lower than in theoretical prediction because of the strong electron trapping in or near the ILs.

In this work, the effects of Al_2O_3 ILs in the ferroelectric characteristics of TiN/$Hf_{0.5}Zr_{0.5}O_2$ (HZO)/Si gate stacks are studied in comparison with SiO_x ILs by the positive-up-negative-down (PUND) measurements. The effects of annealing time and ambient between N_2 and forming gas (FG) are also examined.

Experimental The key process steps of the device fabrication are shown in Fig. 1(a). 1-nm-thick Al_2O_3 was grown on a HF-last pre-cleaned p^+ Si substrates before the deposition of 8.6, 10.2, 11.2, and 12.2-nm HZO by ALD. For comparison, we also prepared capacitors without intentional ILs, where SiO_x ILs has been formed on Si [5], caused by OH-dense atmosphere before the nucleation of HZO [6]. Then, 60-nm TiN was sputtered followed by the thermal evaporation of 100-nm Al as the top electrode. After patterning, annealing for 1 min or 20 min in N_2, or 20 min in FG, was carried out at 400˚C for inducing ferroelectricity.

The ferroelectric characteristics were evaluated by the PUND method with a ±4 V/1k Hz triangular waveform after 100 wake-up cycles with ±4 V/1k Hz.

Results and Discussion Fig. 1(b) shows the relationship between the capacitance-equivalent-thickness (CET) and the physical thickness of the HZO stacks with Al_2O_3 or SiO_x IL. The physical thickness of HZO and CET were determined by ellipsometry and the Q–V measurement, respectively. CET of ILs obtained from the intercept, and the k-values of HZO obtained from the slope, are almost the same between the two types of stacks (5 Å and 23, respectively). Thus, same voltage (±4 V) is used in the following PUND measurements to ensure equal effective electric field (E_{OX}) for the two stacks.

The representative P–V and I–V curves for the 11.2-nm-thick HZO stacks with SiO_x and Al_2O_3 IL are shown in Fig. 2(a). $2P_r$ and $\pm V_C$ extracted for 8.6, 10.2, 11.2, and 12.2-nm thick HZO are shown in Fig.2(b) and (c), respectively. It is found that the capacitors with Al_2O_3 IL consistently show larger $2P_r$ and $|V_C|$. Since CET of the stacks at the given HZO thickness and ILs is almost the same between SiO_x and Al_2O_3 IL, we can conclude that the better ferroelectricity of the gate stacks with Al_2O_3 IL is due to the change of HZO properties, rather than the difference in the voltage divider effect due to ILs [7]. The physical origin of this improvement needs to be further investigated.

The effects of annealing time and ambient for the 12.2-nm-thick HZO stacks with Al_2O_3 and SiO_x IL are shown in Fig. 3(a) and (b), respectively. It is observed that $2P_r$ of the stack with SiO_x IL decreases after long time annealing, while that with Al_2O_3 IL has negligible change. The present phenomenon may be attributable to higher stability against transformation from o-phase to m-phase of HZO for stack with Al_2O_3 IL during long time annealing [4] and/or to suppression of any intermixing between HZO and Si [8] by Al_2O_3 IL as a diffusion barrier. Moreover, it is found that FGA has little impact to capacitors with SiO_x and Al_2O_3 IL.

Conclusion We have demonstrated the improvement of $2P_r$ for the TiN/HZO/Si ferroelectric gate stacks with Al_2O_3 IL in comparison with conventional SiO_x IL. Moreover, higher robustness against long time annealing has also been achieved with Al_2O_3 IL.

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References [1] S. Dunkel *et al., IEDM* (2017) [2] M. Jerry *et al., IEDM* (2017) [3] M. Park *et al., APL* **102**, 242905 (2013) [4] A. Toriumi *et al., IEDM* (2019) [5] K. Toprasertpong *et al., IEDM* (2019) [6] J. Hackley *et al., J. Vac. Sci. Technol. A* **26**, 1235 (2008) [7] K. Ni *et al., IEEE TED* **65**, 2461 (2018) [8] A. Tan *et al., IEEE TED* **39**, 95 (2018)

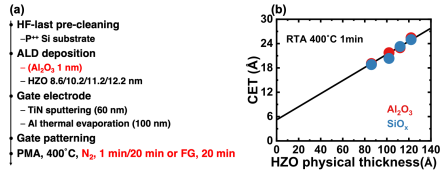

Fig.1: (a) Key process steps for fabricating the devices used in this work. (b) CET as a function of physical thickness of HZO for stacks with Al_2O_3 and unintentional SiO_x IL.

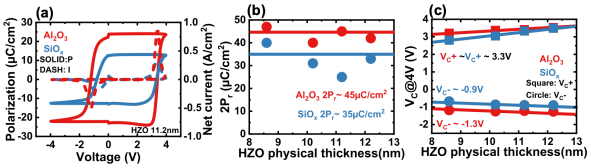

Fig.2: (a) P–V and I–V curves of stacks with Al_2O_3 and SiO_x IL of 11.2-nm-thick HZO. (b) $2P_r$ and (c) V_C as a function of HZO thickness for devices with Al_2O_3 and SiO_x IL.

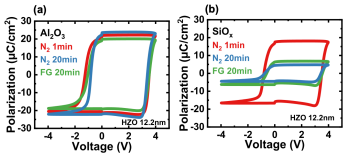

Fig.3: P–V and I–V relationships after annealing for devices with (a) Al_2O_3 and (b) SiO_x IL at the HZO thickness of 12.2-nm.