The low temperature fabrication of gate-first Schottky barrier pMOSFET with PdErSi source and drain

Tokyo Institute of Technology, °R. M. D. Mailig, Y. Aruga, M. G. Kim, and S. Ohmi

E-mail: mailig.r.aa@m.titech.ac.jp, ohmi@ee.e.titech.ac.jp

1. Introduction

The main requirement for the integration of the high-k gate insulators such as HfN or HfO_2 in the gate-first CMOS fabrication is the low-thermal budget process below 500°C. In this case, the Schottky barrier (SB) source and drain (S/D) utilizing metal silicides are replacing the conventional diffusion S/D regions to realize the low temperature process [1]. One of the candidate S/D materials for this process is the PdEr-silicide alloy [2, 3]. It was previously reported that low contact resistivity is achieved by using PdErSi as contact material [3]. In this work, the PdErSi as S/D material in the gate-first SB p-channel MOSFET (pMOSFET) was investigated.

2. Experimental Procedure

The n-Si(100) substrates were cleaned using SPM and DHF. The 180-nm-thick SiO_2 field oxide was formed by wet oxidation at 850°C. Next, the 100x100 μm^2 active regions were patterned by photolithography and wet etching. Next, the channel stop ion implantation of phosphorus dopants was performed with an ion dose of 1×10^{14} cm^2 at 100 keV followed by 900°C/20 min annealing under 1 SLM N_2 ambient in RTA for dopant activation. Then, the 10-nm-thick HfO_2 gate oxide was deposited by RF magnetron sputtering with 2.0/0.2 sccm Ar/O_2 gas, 60 W RF power at 0.35 Pa and room temperature (RT). The 25-nm-thick PdEr encapsulating layer was in-situ deposited at RT with 2.2 sccm Kr, 120 W RF power at 0.7 Pa. Next, the S/D regions were patterned followed by the gate stack annealing at 600°C/30 s using RTA under 1 SLM N_2 ambient. Then, the silicide S/D regions were formed by depositing 20-nm-thick PdEr with 10-nm-thick TiN encapsulating layer using RF magnetron sputtering and by silicidation at 500°C/1 min using RTA under 1 SLM N_2 ambient [2]. The TiN layer was selectively etched by NH_4OH:H_2O_2 (1:1) solution at 45°C. A 10-nm-thick PdEr was deposited after the TiN etching for the contact electrode patterning and etching. Finally, the Al back contact was deposited by evaporation.

3. Results and Discussion

Figure 1 shows the I_D-V_D characteristics of the SB pMOSFET. The PdErSi was successfully integrated as a S/D in the gate-first MOSFET process with the silicidation temperature as low as 500°C. In this regard, the PdErSi S/D formation at 500°C/1 min is much lower than the conventional boron dopant activation annealing at temperatures greater than 900°C. The inset in Fig. 1 shows the actual device with channel length (L) and width (W) equal of 30 µm and 95 µm, respectively.

Figure 2 shows the I_D-V_G characteristics of the SB pMOSFET at $V_D = -1$ V. The parameters of the SB pMOSFET were extracted as threshold voltage $(V_{TH}) = -1$ V, $I_{ON}/I_{OFF} = 1.0 \times 10^2$, and subthreshold swing $(SS) = 290$ mV/dec.

4. Conclusion

The PdErSi alloy silicide was integrated in the gate-first SB MOSFET process with low thermal budget for the first time. As a conclusion, the PdErSi alloy could be used not only as contact material but also as a S/D material in gate-first SB MOSFET process.

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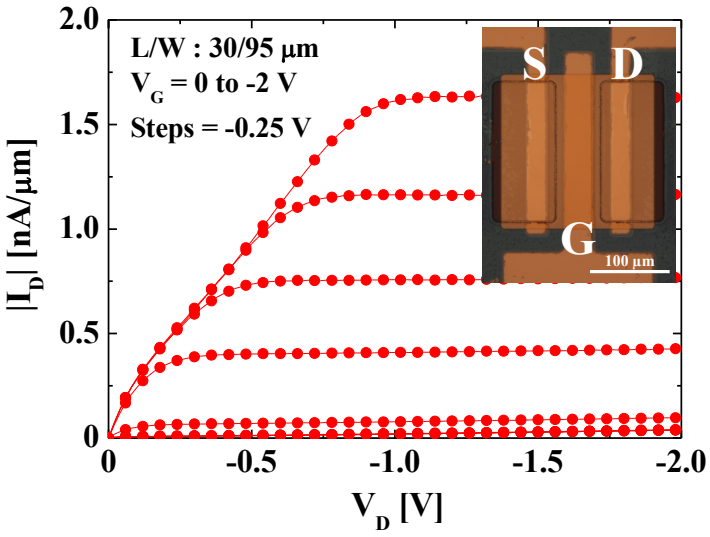

Fig. 1 I_D-V_D of the SB pMOSFET.

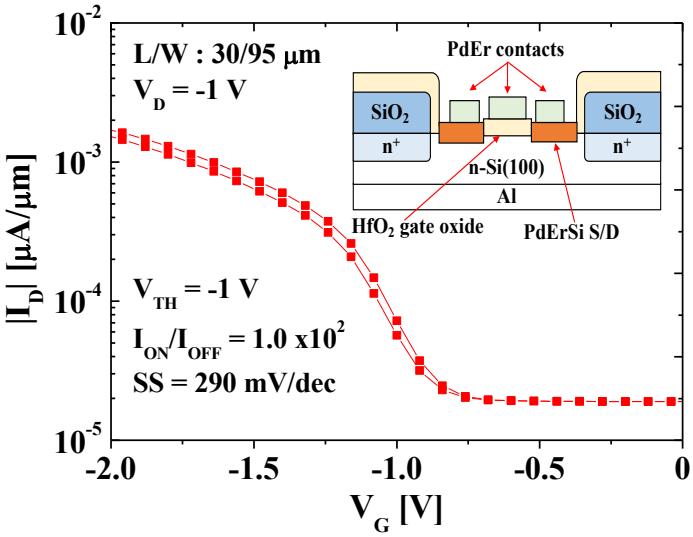

Fig. 2 I_D-V_G of the SB pMOSFET.