1000℃酸素アニールで SiO_2/β-Ga_2O_3 界面に生じる絶縁性 Ga_2O_3 層とその MOS 特性への影響

Insulating Ga_2O_3 layer formation at SiO_2/β-Ga_2O_3 interface during oxygen annealing at 1000℃ and its impact on Ga_2O_3 MOS interface characteristics

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[Introduction] We have demonstrated the formation of SiO_2/β-Ga_2O_3 MOS interface with very low D_{it} (< 10^{11} $cm^{-2}eV^{-1}$) using PDA at 1000℃ in O_2 [1]. On the other hand, it is well known that O_2 annealing at elevated temperatures induces a significant increase of the resistivity of β-Ga_2O_3 surface, by forming thin insulating layer [2], where the effective carrier density is significantly reduced. In this study we investigated the impacts of oxidation-induced insulating β-Ga_2O_3 layer formation at SiO_2/β-Ga_2O_3 interface during high temperature oxygen annealing on the characteristics of the MOS capacitors.

[Experimental] After surface cleaning of β-Ga_2O_3 (001) wafers with n-type epitaxial layers (carrier density ~ 10^{16} cm^{-3}) in 5% HF, SiO_2 films were deposited by electron-beam evaporation of Si in O_2 flow (~ 10^{-2} Pa), followed by PDA in O_2 at 600-1000℃. The XRR (x-ray reflectivity) measurements were employed to determine T_{SiO2} (SiO_2 physical thickness). Au gates were evaporated to fabricate Au/SiO_2/β-Ga_2O_3 (001) MOS capacitors, to determine the CET (capacitance equivalent thickness, defined as $\varepsilon_{SiO2}/C_{max}$) as well as N_d (effective carrier density) from C^{-2}–V relationship under depletion bias.

[Results & discussions] Figure 1 shows T_{SiO2} before and after O_2 annealing for 1hr at 600℃ or 1000℃, respectively. T_{SiO2} (initial T_{SiO2} = 28 nm case) increases a little by 600℃ annealing, which may be explained by a compensation of oxygen deficiency, whereas it does not change even by increasing the temperature up to 1000℃, which indicates there is no significant intermixing of SiO_2 with Ga_2O_3. Meanwhile, according to Fig. 2, CET (initial T_{SiO2} = 52nm case) dramatically increases by extending the annealing duration at 1000℃, or by increasing the annealing temperature. Such anomalous increase of CET is explainable by assuming the surface of Ga_2O_3 becomes insulating due to the O_2 annealing, and contributes as an additional dielectric layer grown under SiO_2. Taking account of higher dielectric constant of Ga_2O_3 (~10) than SiO_2 (~4), the surface region of Ga_2O_3 as thick as ~20 nm would work as insulating layer after 1hr O_2 annealing at 1000℃. Thus the “electrically active” MOS interface may exists deep inside of Ga_2O_3, which may be the reason why we can achieve the superior MOS characteristics by O_2 annealing at 1000℃. At the same time, we also detected the change of the depth profile of N_d, estimated from the C^{-2}-V relationship, as shown in Fig.3. The formation of a lower N_d region in a few hundreds of nanometers near the MOS interface is understandable as another impact of O_2 annealing at 1000℃ on the surface of Ga_2O_3.

[Conclusions] Significant change of carrier density in the surface region of Ga_2O_3 in SiO_2/β-Ga_2O_3 MOS capacitors by O_2 annealing at 1000℃ was indicated to result in both the increase of the effective dielectric layer thickness and the formation of a lower N_d region with the depth of ~ a few hundreds of nanometers. Such change of the interface electrical structure may be related to the formation of MOS interface with significantly reduced D_{it}. This work was partly done in the collaboration with JST-LCS.

References: [1] E. Suzuki et al., 2018 Spring Meeting of JSAP, 12a-M121-5. [2] T. Oshima et al., JJAP 52, 051101(2013).

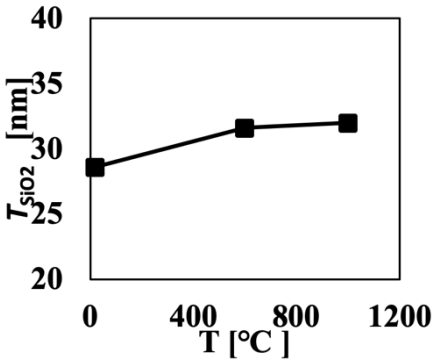

Fig.1 Annealing temperature dependence of T_{SiO2} during 1hr O_2 annealing.

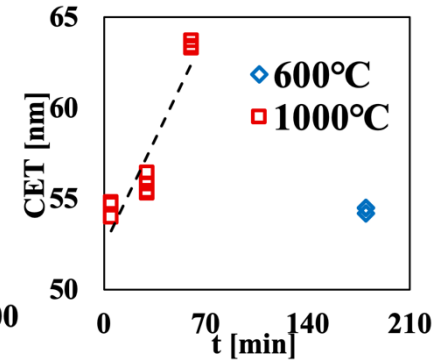

Fig.2 O_2 Annealing duration dependence of CET for 1000℃ and 600℃.

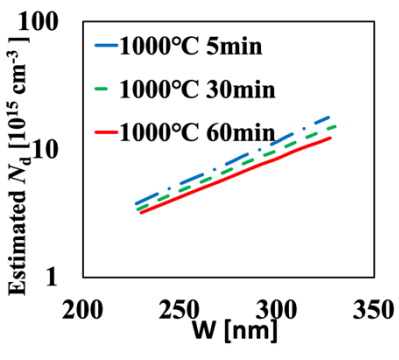

Fig.3 Estimated profile of N_d of capacitors fabricated by annealing at 1000℃ with various durations.