High-frequency Response of Si-SET: Experimental Verification

○Alka Singh[1], Tomoki Nishimura[2], Hiroaki Satoh[2,3], Hiroshi Inokawa[1,2,3]

GSST, Shizuoka Univ. [1], GSIST, Shizuoka Univ. [2], RIE, Shizuoka Univ.[3]

E-mail: inokawa.hiroshi@shizuoka.ac.jp

1. Introduction

It has been observed that there is no upper limit of frequency in the rectifying operation of single-electron transistors (SETs) [1]. Theoretical explanation behind this is that the asymmetry in the tunneling rate with respect to drain voltage is responsible for asymmetry in the drain current, resulting in rectification even at higher frequency beyond the conventional cutoff frequency [2]. Here, the details of ongoing experimental verification are reported.

2. Experimental setup

Devices under consideration are i) SET by PADOX method (Fig. 1), and ii) heavily doped Si nanowire-base SET (Fig. 2). In addition, reference Schottky barrier diode is used to calibrate the measurement system. Frequency response of SET placed inside the low-temperature (LT) chamber is measured by applying high-frequency signal from Agilent N5181A signal generator (100 kHz ~ 3 GHz) to the drain terminal via GSG probe and 6dB attenuator for providing DC return path (Fig. 3).

3. Calibration of measurement system

Signal generator along with GSG probe and LT chamber has been calibrated to obtain flat frequency response (Fig. 4). After the calibration, actual measurement will be performed to get the expected frequency response of SET.

Reference: [1] Y. Takahashi, et al. ECS Transactions, 58 (9) 73-80 (2013).

[2] H. Inokawa, et al., IEEE EDSSC (Shenzhen, China, Jun. 6-8, 2018).

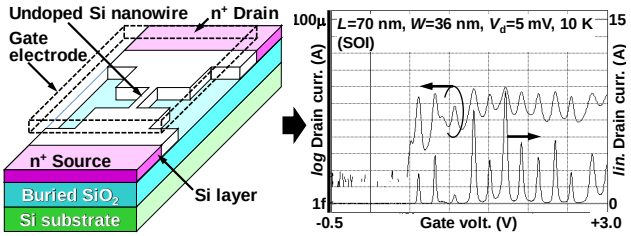

Fig. 1 Schematic diagram and transfer characteristics of SET by PADOX method.

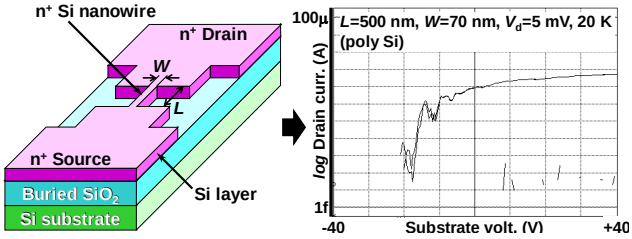

Fig. 2 Schematic diagram and transfer characteristics of heavily doped Si nanowire-based SET.

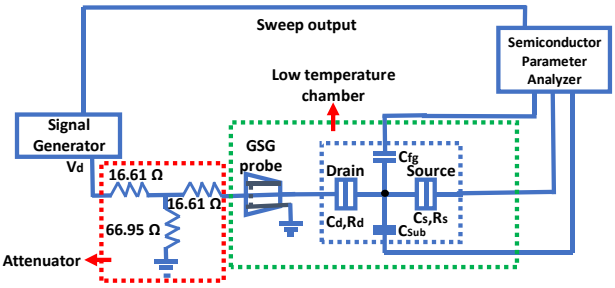

Fig. 3 High-frequency measurement setup.

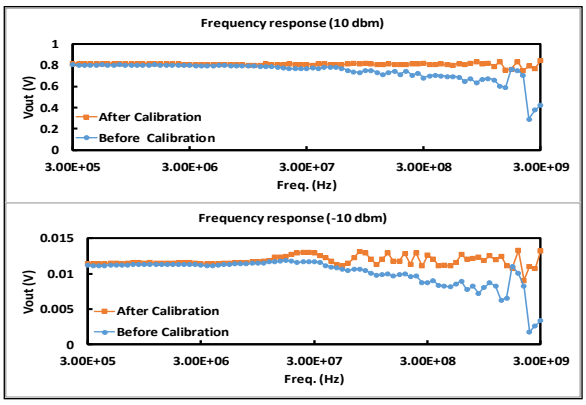

Fig. 4 Frequency response of the measurement system before and after the calibration.