プラズマ酸化により作製したAl_2O_3/GeO_x/n-Ge MOS 界面における遅い準位の特性

Characteristics of slow traps in Al_2O_3/GeO_x/n-Ge MOS interfaces by plasma oxidation

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Introduction One of the key technologies for realizing Ge CMOS is the formation of gate stacks with low defect densities. In order to reduce fast interface states, (HfO_2)/Al_2O_3/GeO_x/Ge interfaces realized by post plasma oxidation (Post-PO) are promising [1, 2]. However, a remaining critical issue is the existence of a large amount of slow traps [3-5], which can be an inherent problem for Ge gate stacks.

Experiments The first structure have 1.5-nm-thick Al_2O_3 by ALD at 300ºC, followed by ECR post-PO. The second sample has pre-PO GeO_x, followed by 1.5-nm-thick Al_2O_3 ALD at 300ºC. PDA was performed for 30 min at 400 ºC in N_2 ambient, followed by 100-nm-thick Au gate electrodes [7-8].

Results and Discussions Recently, a simple and effective method to estimate the slow trap areal density (N_{st}) responsible for BTI reliability from MOS capacitors has been proposed [4, 5]. Fig. 1(a) schematically shows the measurement procedure and the experimental results. Here, V_g is repeatedly scanned between the minimum voltage (V_{start}) and the maximum voltage (V_{stop}), with increasing V_{stop}. The amount of slow trap density responding to this scan (ΔN_{st}) can be estimated from the amount of hysteresis (ΔV_{hys}) in the C-V measurement with forward and backward scans as a function of the maximum effective electric field across gate insulators (E_{ox}). Here, E_{ox} and ΔN_{st} can be given by $E_{ox} = |V_{stop} - V_{FB}|/CET$ and $q\Delta N_{st} = C_{ox}\Delta V_{hys}$ on the assumption that all traps locate very close to the MOS interfaces. Fig. 1(b) shows V_{FB} values in the forward and back scan, extracted from Fig. 1(a), as a function of E_{ox}. It is confirmed that V_{FB} in the backward scan keeps increasing, while V_{FB} in the forward scan almost no change under the present low E_{ox}, meaning that only electron trapping and no hole trapping occur. It is verified, as a result, that the amount of electrons trapped in slow states increases with an increase in E_{ox}, because the difference of V_{FB} in the forward and backward scan corresponds to ΔV_{hys} and resulting ΔN_{st}. Next, the influence of the C-V scan time is examined. Here, the hold time at the V_{min} and V_{max} points during C-V measurements is varied under constant V_{min} and V_{max} values. Fig. 2 show the C-V curves with changing the V_{start} and V_{stop} hold times. The C-V curves have no change with changing the V_{start} hold time, meaning that the occupancy of slow traps at V_{FB} in the forward scan is under the equilibrium condition. On the contrary, when the V_{stop} hold time increases, ΔV_{hys} becomes larger. Since V_{FB} only in the backward scan increases, the total amount of trapped electrons increases with the time and there is no saturation in ΔN_{st}. These results indicate that the time constant of electron trapping into slow traps is widely distributed and that traps with very long time constants exist.

In order to carefully examine the difference in ΔN_{st} of n-Ge between the pre- and post-PO process [8], ΔN_{st} is evaluated by C-V curves with changing the step time, which is the waiting time at each V_g step, shown in Fig. 3(a). It is confirmed that ΔN_{st} is higher in the post-PO capacitors, irrespective of the step time, indicating that the difference in ΔN_{st} between the pre- and post-PO process is attributed to the difference in the total slow trap density, not to the modulation of the time constant. Fig. 3(b) shows a schematic model to explain the increase in slow traps by the post-PO process. We can interpret that additional slow traps can be generated by the post-PO process, independent of the defects inherent to GeO_x, probably through any reaction and/or inter-diffusion between Al_2O_3 and GeO_x.

Conclusion We have carefully studied the electron slow trap density in Al_2O_3/GeO_x/n-Ge MOS interfaces with plasma oxidation by C-V hysteresis measurement. It has been found that electron trapping can be qualitatively understood by trap distributions spread widely along both the energy and the depth directions and a large amount of additional slow traps are generated very close to GeOx/Ge interfaces by post-PO.

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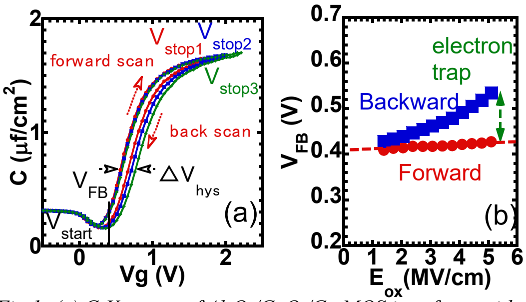

Fig.1: (a) C-V curves of Al_2O_3/GeO_x/Ge MOS interfaces with changing V_{stop} (b) V_{FB} values for C-V scans

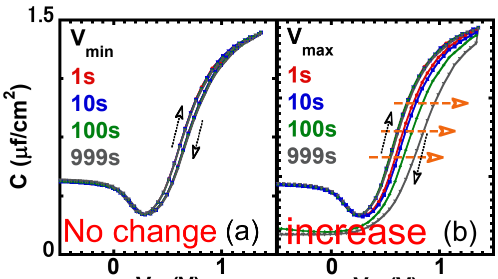

Fig.2: C-V curves with different (a) V_{min} and (b) V_{max} hold time

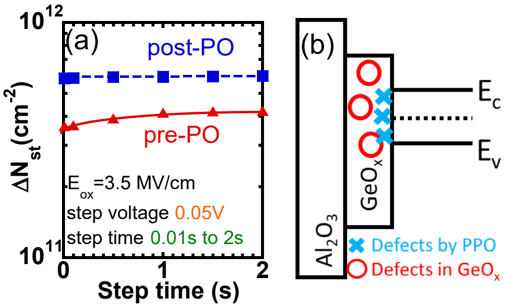

Fig.3: (a) Slow trap density as a function of step time in Ge MOS interfaces with post-PO and pre-PO. (b) Schematic diagram for slow trap generation by the post-PO process.