n-Ge MOS 絶縁膜中の異なるキャリア捕獲トラップの峻別手法の提案

Proposal of a measurement method to discriminate different types of traps in n-Ge MOS gate insulators

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Introduction To improve the reliability of Ge gate stacks, understanding of slow trap characteristics in Ge MOS interfaces is extremely important [1-3]. We have applied the conventional method to estimate ΔN_{st} in n-Ge MOS interfaces [3]. Here, hysteresis observed in the C-V scan with low V_{stop} (E_{ox}) is attributed to electron trapping into existing slow trap sites. In this study, we propose a new measurement scheme to discriminate pre-existing, generated electron slow traps and hole traps under electrical stress and apply this method to Al_2O_3/GeO_x/n-Ge with PPO MOS interfaces [6]. It is found that, when higher V_{stop} (E_{ox}) is applied, both hole trapping and generation of new electron slow traps occur.

Experiments After pre-cleaning, 1.5-nm-thick Al_2O_3 was deposited at 300°C by ALD on n-Ge. Subsequently, plasma post oxidation was performed by using ECR plasma of Ar (9 sccm) and O_2 (3 sccm) at 300 °C under 650 W RF power for 10 s. PDA was performed for 30 min at 400 °C in N_2 ambient, followed by formation of 100-nm-thick Au gate electrodes and Al back contacts by thermal evaporation.

Results and Discussions Fig. 1(a) shows that the C-V curves have no change under V_g repeated scan, where E_{ox} is small. However, when E_{ox} increased up to values higher than a critical one ($E_{critical}$), V_{FB} starts to shift toward negative V_g direction (Fig. 1(b)), which is different from the C-V curves under small E_{ox}. The negative V_{FB} shift in the forward scan increases with an increase in the cycle number, suggesting the increase in the amount of trapped holes, which has been reported in Ge p-MOSFETs after NBTI stress [4, 5]. The present phenomenon can be explained by a model of Fig. 2. Under low E_{ox}, only electrons in Ge are trapped into slow traps during C-V measurements. Under high E_{ox}, on the other hand, hot holes created probably in the gate metal are injected into dielectrics and trapped into hole traps. These trapped holes do not come out, once trapped, and cause the negative V_{FB} shift as fixed positive charges. In addition to hole trapping, we have found that generation of slow electron traps occurs at E_{ox} higher than $E_{critical}$. In order to discriminate generated and existing electron slow traps, we propose a new measurement in Fig. 3. Here, after applying high V_{stop} once, ΔV_{hys} under the initial C-V scan condition with sufficiently low V_{stop} is re-measured. Since ΔV_{hys} does not change for the repeated measurements with low V_{stop}, the increment ΔV_{hys} corresponds to ΔN_{st} for generated slow traps. We can discriminate and determine $\Delta N_{st\text{-}total}$, $\Delta N_{st\text{-}generated}$, $\Delta N_{st\text{-}existing}$ (total, generated, existing electron slow traps density), and ΔN_h (hole traps density) under the proposed measurement as follows;

$$\Delta N_{st-total} = \Delta V_{hys2} \times C_{ox}/q,$$
$$\Delta N_{st-generated} = (\Delta V_{hys1} - \Delta V_{hys0}) \times C_{ox}/q,$$
$$\Delta N_h = \Delta V_{forward} \times C_{ox}/q,$$
$$\Delta N_{st-existing} = \Delta N_{st-total} - \Delta N_{st-generated}$$

Fig. 4 shows these densities in the Al_2O_3/GeO_x/Ge MOS interfaces with post-PO. It is found that $\Delta N_{st\text{-}existing}$ dominates $\Delta N_{st\text{-}total}$ in lower E_{ox}, while $\Delta N_{st\text{-}generated}$ is comparable to or higher than $\Delta N_{st\text{-}existing}$ in higher E_{ox}. Also, ΔN_h is comparable to $\Delta N_{st\text{-}existing}$ and $\Delta N_{st\text{-}generated}$ in high E_{ox}.

Conclusion We have proposed a new evaluation method to discriminate the different types of slow traps in Ge nMOS interfaces in large E_{ox}. It was found that only existing slow traps are responsible in low E_{ox}, while generation of slow traps and hole trapping additionally occur in high E_{ox}.

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References [1] R. Zhang et al., IEDM (2011), 642 [2] M. Ke et al., APL (2016) [3] G. Groesenken et al., IEDM (2014) 828 [4] J. Ma et al., MEE 109 (2013) 43 [5] J. Ma et al., TED 61 (2014) 1307 [6] M. Ke et al, IEDM 791(2018)

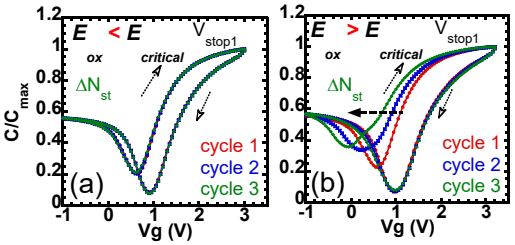

Fig.1: C-V curves under cycle scans with same V_{start}, and (a) V_{stop} is smaller than $V_{critical}$, (b) V_{stop} is larger than $V_{critical}$.

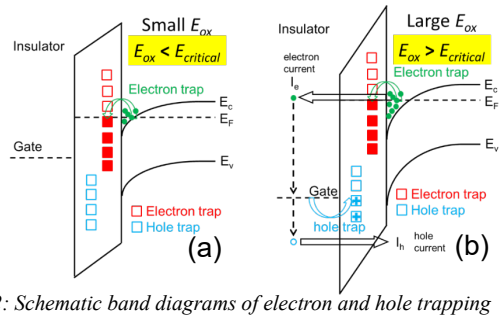

Fig.2: Schematic band diagrams of electron and hole trapping behaviors under (a) low E_{ox} and (b) high E_{ox} in n-MOS gate stacks.

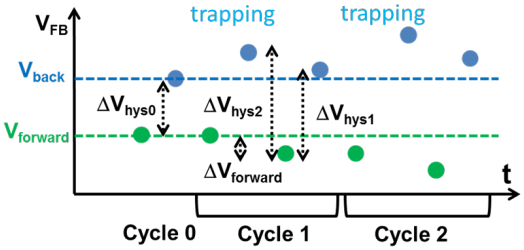

Fig.3: Schematic view of V_{FB} change in forward and backward scan for evaluating the density of existing and generated slow electron trap density and hole trap density as a function of E_{ox}.

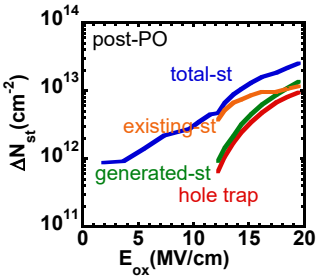

Fig.4: Total, generated and existing electron slow trap density, and hole trap density of Al_2O_3/GeO_x/Ge MOS interface with post-