n-Ge MOS 構造における異なる界面層へのキャリアトラップ特性の比較

Comparison of carrier trap characteristics in different interfacial layers of n-Ge MOS structures

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Introduction One of the key technologies for realizing Ge CMOS is the formation of gate stacks with low defect densities. $(HfO_2)/Al_2O_3/GeO_x/Ge$ interfaces realized by post plasma oxidation (post-PO) are promising for reducing interface states density [1, 2]. However, a remaining critical issue is the existence of a large amount of slow traps [3-5], which can be an inherent problem for Ge gate stacks. It has been reported that Y-doped GeO_x interfaces and $Al_2O_3/GeO_x/Ge$ formed by pre plasma oxidation (pre-PO) can reduce slow trap density (N_{st}) [6-8]. However, reduction in N_{st} is not sufficient yet, particularly for electrons. Thus, understanding of physical origins of the slow electron traps and the carrier trapping properties is strongly required to establish a guideline for further reduction in N_{st} and a method of the oxide reliability prediction for Ge MOS interfaces. We have proposed a new measurement to discriminate existing and generated electron slow traps [9]. It has been found that only existing slow traps are responsible in low E_{ox}, while generation of slow traps and hole trapping additionally occur in high E_{ox}. In this study, we compare the existing electron, generated electron and hole trap density of n-Ge MOS interfaces with different interfacial layers including Y_2O_3 under electrical stress by utilizing the above technique.

Experiments Fig. 1 shows the process flows of fabricated MOS structures. The first and third structures have 1.5-nm-thick Al_2O_3 only and 0.7-nm-thick Y_2O_3, 1.5-nm-thick Al_2O_3 by ALD at 300°C, respectively, followed by ECR post-PO. The second sample has pre-PO GeO_x, followed by 1.5-nm-thick Al_2O_3 ALD at 300°C. PDA was performed for 30 min at 400 °C in N_2 ambient, followed by 100-nm-thick Au gate electrodes [7, 8].

Results and Discussions Fig. 2 shows the comparison of $\Delta N_{st\text{-}total}$, $\Delta N_{st\text{-}existing}$, $\Delta N_{st\text{-}generated}$ (total, generated, existing electron slow traps density) and ΔN_h (hole traps density) among the post- and pre-PO Al_2O_3/GeO_x/n-Ge, and post-PO $Al_2O_3/Y_2O_3/GeO_x$/n-Ge gate stacks, evaluated by the proposed method [9]. It is found that $\Delta N_{st\text{-}existing}$ in high E_{ox} is almost the same, while pre-PO exhibits the lowest $\Delta N_{st\text{-}existing}$ value in low E_{ox}, attributed to the process free from electron trap generation by post-PO. Also, $\Delta N_{st\text{-}generated}$ is almost the same between pre- and post-PO $Al_2O_3/GeO_x/Ge$. These facts suggest that the generation of slow electron traps in high E_{ox} are determined by a common nature of pure GeO_x. It is found, on the other hand, that $Al_2O_3/Y_2O_3/GeO_x/Ge$ shows much lower ΔN_h and $\Delta N_{st\text{-}generated}$, meaning that insertion of Y_2O_3 and doping of Y into GeO_x can be an effective way to improve the gate stack reliability in high E_{ox}. This result is consistent with the report on stabilization of GeO_2 network by Y incorporation [10]. As a result, we can interpret that lower $\Delta N_{st\text{-}total}$ of pre-PO in low E_{ox} and $Al_2O_3/Y_2O_3/GeO_x/Ge$ in high E_{ox} are attributed to the suppression of existing trap generation due to pre-PO and the increased robustness against electron slow trap generation and hole traps, respectively. The present analyses also suggest that existing and generated electron slow trap/hole traps have the different physical origins.

Conclusion We used a new method to evaluate the densities of existing, generated electron slow trap and hole trap density for $Al_2O_3/Y_2O_3/GeO_x$/n-Ge MOS interfaces with post-PO and Al_2O_3/GeO_x/n-Ge MOS interfaces with post- and pre-PO. The pre-PO and Y_2O_3 insertion have been found to reduce existing and generated slow electron traps, respectively, contributing to the reduction in total slow trap density.

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References [1] R. Zhang et al., APL 98 (2011) 112902 [2] R. Zhang et al., TED 60 (2013) 927 [3] R. Zhang et al., IEDM (2011), 642 [4] J. Franco et al., IEDM (2013) 397 [5] G. Groesenken et al., IEDM (2014) 828 [6] C. Lu et al., JAP 116 (2014) 174103 [7] M. Ke et al., MEE 178 (2017), 132 [8] M. Ke et al., ESSDERC (2017) 296 [9] M. Ke et al., IEDM (2018) 791 [10] C. Lu et al., IEDM (2015) 370

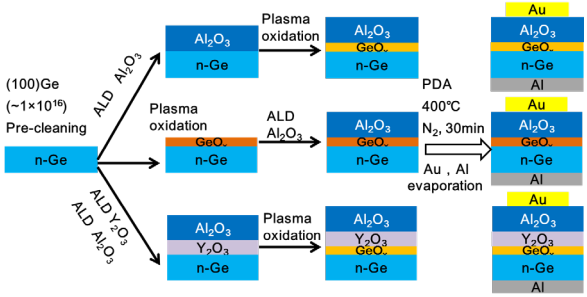

Fig. 1: Process flow and structures for and $Al_2O_3/GeO_x/Ge$ with post-PO, $Al_2O_3/GeO_x/Ge$ with pre-PO and $Al_2O_3/Y_2O_3/GeO_x/Ge$ with post-PO MOS interfaces.

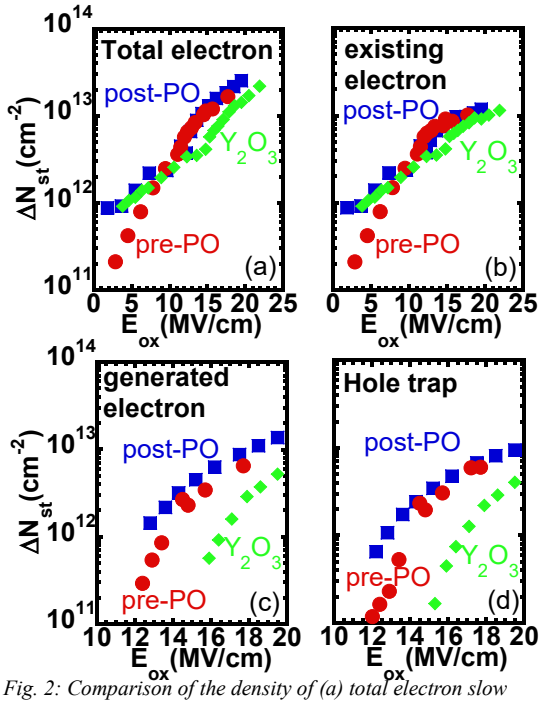

Fig. 2: Comparison of the density of (a) total electron slow traps, (b) existing electron slow traps, (c) generated electron slow traps and (d) hole traps in $Al_2O_3/GeO_x/Ge$, $Al_2O_3/Y_2O_3/GeO_x/Ge$ gate stacks with post-PO and $Al_2O_3/GeO_x/Ge$ gate stacks with pre-PO.